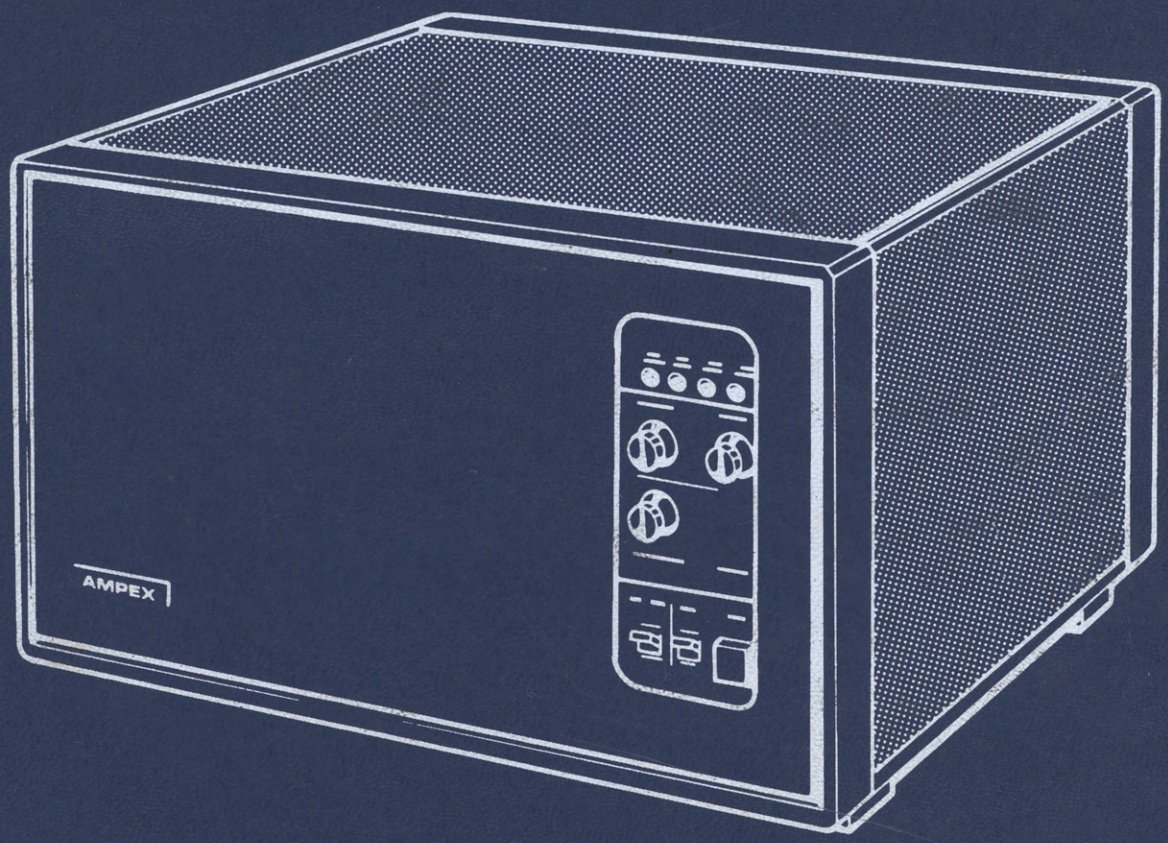
TBC-2B

DIGITAL TIME-BASE CORRECTOR

(NTSC)



THEORY AND MAINTENANCE

1809474

AMPEX

Catalog No. 1809474-01
Issued: August 1981
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TBC-2B

DIGITAL TIME-BASE CORRECTOR

(NTSC)

DESCRIPTION AND MAINTENANCE

AMPEX CORPORATION
AUDIO-VIDEO SYSTEMS DIVISION

Prepared by

AVSD Technical Publications
Ampex Corporation
401 Broadway
Redwood City, CA 94063

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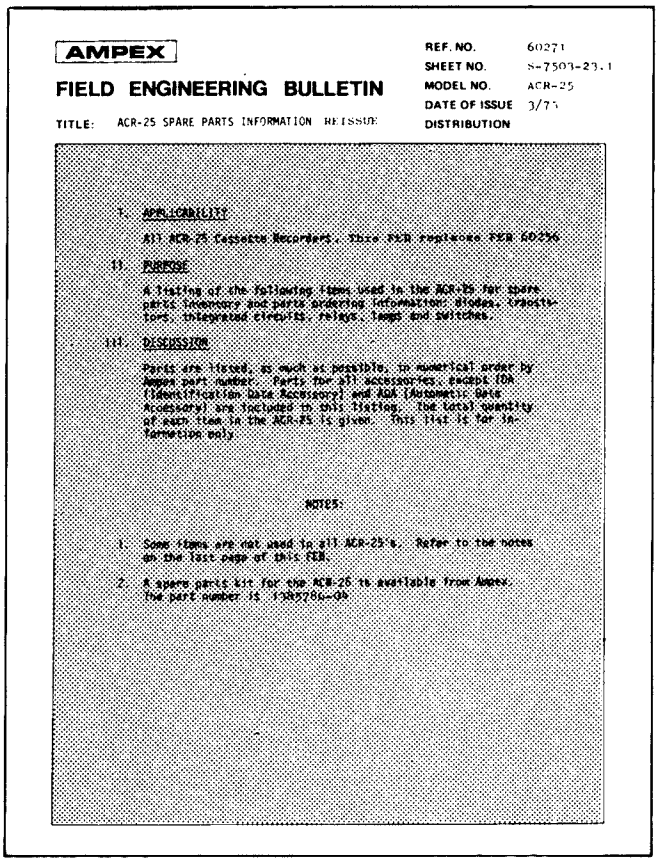
FOR ADDITIONAL TECHNICAL INFORMATION

FIELD ENGINEERING BULLETIN SERVICE



AMPEX

FIELD ENGINEERING BULLETIN

TITLE: ACR-25 SPARE PARTS INFORMATION REISSUE

REF. NO. 60271
SHEET NO. S-7503-23.1
MODEL NO. ACR-25
DATE OF ISSUE 3/75
DISTRIBUTION

I. APPLICABILITY

All ACR-25 Cassette Recorders. This FEB replaces FEB 60256

II. PURPOSE

A listing of the following items used in the ACR-25 for spare parts inventory and parts ordering information: diodes, transistors, integrated circuits, relays, lamps and switches.

III. DISCUSSION

Parts are listed, as much as possible, in numerical order by Ampex part number. Parts for all accessories, except TDA (Identification Data Accessory) and ADA (Automatic Data Accessory) are included in this listing. The total quantity of each item in the ACR-25 is given. This list is for information only.

NOTES:

1. Some items are not used in all ACR-25's. Refer to the notes on the last page of this FEB.
2. A spare parts kit for the ACR-25 is available from Ampex. The part number is 1305786-04

THE AMPEX AUDIO-VIDEO SYSTEMS DIVISION'S TECHNICAL SUPPORT GROUP PUBLISHES FIELD ENGINEERING BULLETINS (FEBs) DESCRIBING APPROVED EQUIPMENT MODIFICATIONS, SPECIAL TOOLS AND ACCESSORIES PLUS INFORMATION ON IMPROVED OPERATING AND MAINTENANCE TECHNIQUES.

TO RECEIVE THESE BULLETINS, SEND US THE FOLLOWING INFORMATION:

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Serial No. **Dealer's Name** **Dealer's Address**

Date of Purchase

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Audio-Video Systems Division, Technical Support Group
401 Broadway, Mail Stop 3-46
Redwood City, California 94063

OUTSIDE UNITED STATES TO:

YOUR NEAREST SALES AND SERVICE COMPANY

(ADDRESSES ON REAR OF THIS PAGE)

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FRANCE
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92100 Boulogne
France

GERMANY (Federal Republic)
Ampex Europa GmbH
6000 Frankfurt, (Main)
Walter-Kolb-Str. 9-11
Germany (Federal Republic)

GREECE
Ampex World Operations S.A.
32 Kiffissias Avenue
P.O. Box 45, Paradissos
Athens, Greece

HONG KONG
Ampex World Operations S.A.
1801-1805 Star House
8 Salisbury Road
Kowloon, Hong Kong B.C.C.

ITALY
Ampex Italiana S.p.A.
Via Riccardo Gigante, 4
00143 Roma
Italy

JAPAN
Ampex Japan Ltd.
3, Kojimachi 3-Chome
Chiyoda-Ku
Tokyo, Japan 102

MEXICO
Ampex De Mexico, S.A. de C.V.
Apartado Postal 13-615
Division del Norte No. 1832
Mexico 13, D.F.

NETHERLANDS
Ampex B.V.
3506 Utrecht
Zamenhofdreef 65A
Netherlands

PUERTO RICO
Ampex Pan American Co.
Edificio San Miguel Hermanos
Oficinas 412 y 413
Avenida Kennedy 1880
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101 Cecil St.
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SPAIN
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Madrid 33, Espana

SWEDEN
Ampex A.B.
Rissneleden 8
P.O. Box 7056
S-172 07 Sundyberg
Sweden

SWITZERLAND
Ampex World Operations S.A.
1701 Fribourg
Rue de Romont 29
P.O. Box 1031
Switzerland

UNITED KINGDOM
Ampex Great Britain Ltd.
Acre Road
Reading, Berkshire RG2 0QR
England

UNITED STATES
Ampex International
401 Broadway
Redwood City, CA 94063

AMPEX CORPORATION
AUDIO-VIDEO SYSTEMS DIVISION
401 BROADWAY
REDWOOD CITY, CALIFORNIA 94063
(415) 367-2011

Effective: 1 October 1980

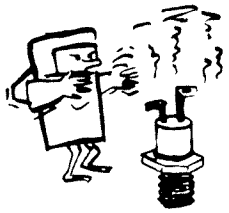
SAFETY AND FIRST AID SUGGESTIONS

Regardless of how well electrical equipment is designed, personnel can be exposed to **dangerous electrical shock** when protective covers are removed for maintenance or other activities. Therefore, it is incumbent on the user to see that all safety regulations are consistently observed and that each individual assigned to the equipment has a clear understanding of first aid related to electrical hazards.

In addition, the following safety practices must be followed:

1 Do not attempt to adjust unprotected circuit controls or to dress leads with power **on**.

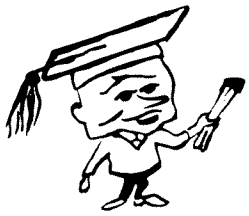
2 Do not touch heavily loaded or overheated components without precaution to avoid burns.



3 Do not assume that all danger of electrical shock is removed when power is off. Charged capacitors can retain dangerous voltages for a long time after power is removed. These capacitors should be discharged through a suitable resistor before any circuit points are touched.

4 Always avoid placing parts of the body in series between ground and circuit points.

5 Remember that some semiconductor cases and solid-state circuits carry high voltages.



6 Don't take chances. Be fully trained. Ampex equipment should be operated and maintained only by fully qualified personnel.

If someone seems unable to free himself while receiving an electrical shock, **turn power off** before attempting to render aid. A muscular spasm or unconsciousness can make a victim unable to free himself from the electrical power.

WARNING

DO NOT
TOUCH VICTIM OR HIS CLOTHING BEFORE
POWER IS REMOVED OR YOU MAY ALSO
BECOME A SHOCK VICTIM

If power cannot be removed immediately, **very carefully** loop a length of dry nonconducting material (such as rope, insulating material, or clothing) around the victim and pull him free of the power. Carefully avoid touching him or his clothing until free of power. Immediately start the appropriate first aid procedures.

GOOD PRACTICES

In maintaining the equipment covered in this manual, please keep in mind the following standard good practices:

1. When connecting any instrument (oscilloscope, waveform monitor, etc.) to a high-frequency output, use the appropriate termination resistor at the input of the instrument, unless the instrument is terminated internally.

2. When inserting or removing printed wiring assemblies (PWAs), cable connectors, or fuses, always turn off power to the affected portion of the equipment. After power is removed, allow sufficient time for the power supplies to bleed down before reinserting PWAs.

3. When troubleshooting, remember that FETs and other metal-oxide-semiconductor (MOS) devices may appear defective because of leakage between traces or component leads on the printed wiring board. Clean the printed wiring board and recheck the MOS device before assuming it is defective.

4. When replacing MOS devices, follow standard practices to avoid damage caused by static charges and soldering.

5. When removing components from PWAs (particularly ICs), use care to avoid damaging PWA traces.

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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PART I

SYSTEM LEVEL

DESCRIPTION AND MAINTENANCE

SECTIONS 1 THROUGH 3

14407-5

TBC-2B Digital Time-Base Corrector

SECTION 1

INTRODUCTION AND SYSTEM HARDWARE

1-1. SCOPE AND ORGANIZATION

This manual has two parts: Part I covers system level description and maintenance; Part II presents description and maintenance information at the printed wiring assembly (PWA) level.

Part I of the manual has three sections: (1) System Hardware, (2) System Description, and (3) System Maintenance. The hardware section illustrates mechanical elements and summarizes major system components and power, signal, and control elements. Section 2 presents a system-level theory which emphasizes the inter-relationships among the PWA's. The system maintenance section introduces a general maintenance plan for the TBC and presents a series of summaries and adjustments which on the one hand repeat information from the *Installation and Operation* manual but which also serve to index control functions seen at the system level to circuit functions at the PWA level.

Part II of the manual presents each PWA in a separate section which includes (1) theory, (2) maintenance procedures, and (3) reference data. Each section number in Part II corresponds to the numerical position of the PWA in the card rack. The reference data is at the end of each section and supports both the description and maintenance texts with block diagrams, simplified schematics, timing waveforms, and other maintenance data.

1-2. RELATED PUBLICATIONS

This manual is the theory and maintenance volume of the TBC-2B manual complement which includes:

- *TBC-2B Digital Time-Base Corrector, General Information, Installation, and Operation,* Catalog No. 1809503.
- *TBC-2B Digital Time-Base Corrector, Parts Lists and Schematics,* Catalog No. 1809485.

This volume supersedes maintenance information contained in the Service Data Package. The *Installation and Operation* and *Parts Lists and Schematics* manuals remain the source of operator information and documentation.

1-3. TBC-2B APPLICATION

The TBC-2 is a color television time-base correction system designed for use with color or monochrome nonsegmented helical-scan videotape recorders with or without a capstan servo (when equipped with the video processor accessory). Ampex capstan-servoed recorders in this category include the recent VPR series (VPR-1, -2, -2B, and VPR-20), and VPR-5100E, VPR-5200, VPR-5800, VPR-7800, and VPR-7900. The TBC-2 may also be used with capstan-servoed or noncapstan-servoed 3/4-inch U-standard cassettes (VPR 4400 and VPR 8300) and 1/2-inch EIAJ-format VTR's.

1-4. TBC-2B SYSTEM HARDWARE

1-5. Physical Description

The basic TBC assembly consists of a standard 19-card rack with up to fifteen printed wiring assemblies (PWA's) with power supply and control panel on the right side. Three views of the system are shown in Figure 1-1 along with lists of the hardware break-out of the major sub-assemblies and options.

1-6. Options and Accessories

Refer to the options list on Figure 1-1. The color processor and video processor are used for heterodyne and non-servoed capstan VTR's, but the color processor also contains chroma inverter circuits necessary for VPR slow-motion operation. Of interest here for the cabinet options is that the console version has a remote control panel which duplicates the standard rack control panel except that the bypass and heterodyne switches remain on the card rack panel. The dropout compensator and velocity compensator options include the S/P and P/S converter functions and replace the basic S/P and P/S converters in the rack. Included in the field accessories is an extender board necessary for field testing. Consult the *Parts Lists and Schematics* manual for more detail on the options and accessories. This manual assumes all the options are integrated into the system and the system is described and tested in those terms.

1-7. Fuse, Power, and Signal Connections

The fuse, power, and signal data is tabulated with illustrations for quick reference in Figure 1-2. All connections are made at the rear panels as shown. Consult the *Installation and Operation* manual for detail on installation. The panel markings for fuse size and use are self-explanatory but note that the +5 Vdc supply fuse is mounted on the inside of the hinged heat sink. The 115/230-power jumper range chart is also printed on the chassis.

1-8. Maintenance Access

Figure 1-3 is a maintenance access diagram which provides a step-by-step procedure for the disassembly of the TBC-2B to the major component level. Each step corresponds to the hardware or component being handled and is also the callout number on the related illustration. When complete disassembly is not required, the table at the upper right of the access diagram lists those steps required to gain access to a particular component.

There are slight differences in the rear support brackets between the cabinet version and the rack mount version of the TBC-2. The console versions do not have the rear support brackets. Except for steps (5) and (6), the disassembly is the same for that shown in the Maintenance Access Diagram.

1-9. SYSTEM CONTROLS AND INDICATORS

For standard operation no routine adjustments need be made beyond the initial setup of the unity trim controls at the top of the control panel for video level, black level, and chroma phase. However, a wider range of tape and facility conditions may be accommodated with the control panel and PWA edge controls. These are summarized in Figure 1-4.

Standard operation in this manual is defined with reference to proposed SMPTE Standard RS170A for video signal definitions (presented in Section 2, *System Description)* with special emphasis on burst/sync phase on color field one for reliable color framing. If tape and reference video conform to standard RS170A video, adjustments to the TBC during recording sessions are minimal.

1-10. Control Panel Controls and Indicators

The control panel operator controls outlined in Figure 1-4 compensate for minor variations from standard tape and facility reference.

1-11. PWA Edge Controls and Indicators

Several of the PWA edge controls extend the flexibility of the TBC to maintain correction under non-standard conditions while other edge controls are factory-set for basic TBC alignment and are on the PWA edge for stability and accuracy of adjustment not possible with the PWA on the extender.

NOTE

As a general rule, assume that the extender should not be used when any edge controls are adjusted.

All edge controls are summarized in Figure 1-4 in terms of the conditions for adjustment and with

references to the appropriate context for adjustment at the system or PWA maintenance level.

1-12. Jumpers

Jumpers on the PWA's fall into two categories: test jumpers and configuration jumpers. Most of the jumpers are related to various testing modes and are called out in the test procedures. These jumpers provide the means to conveniently set up test conditions for troubleshooting, isolation of circuits for alignment, and testing circuit performance. In the event of difficulty, verify that the jumpers are in their "normal" position as listed in Table 1-1. A jumper list is also provided on each PWA-level maintenance data sheet.

The configuration jumpers are called out in the installation procedures for various VTR's in the *Installation and Operation* manual.

Table 1-1. Test and Configuration Jumpers

PWA	JUMPER	POSITION	FUNCTION
2 Color Processor Assy. 1405143 (all versions)	J1		
		A-B	Normal
		B-C	Test—fixed error voltage to crystal oscillator
	J2		
		A-B	Normal
		B-C	Test—removes R-Y encoder
			NOTE: **J3, J4, J5, J12, and J13 are not used.**
	J6		
		A-B	Normal
		B-C	Test—removes B-Y encoder
	J7		
		A-B	Normal
		B-C	Test—luminance low-pass filter alignment
	J8		
		A-B	Normal
		B-C	Test—luminance low-pass filter alignment
	J9		
		A-B	Normal
		B-C	Test—luminance low-pass filter alignment
	J10		
		A-B	Normal
		B-C	Test—luminance low-pass filter alignment
	J11		
		A-B	Normal
		B-C	Test—luminance low-pass filter alignment
	J12		Not used
	J13		Not used
	J14		
		A-B	Normal
		B-C	Test—remove chroma inverter
	J15		
		A-B	Normal
		B-C	Test—chroma invert delay filter alignment
	J16		
		A-B	Normal
		B-C	Test—chroma invert delay filter alignment

Table 1-1. Test and Configuration Jumpers (Continued)

PWA	JUMPER	POSITION	FUNCTION
3 Video Input Assy. 1405134	J1		
		Removed	Normal
		A–B	Low-pass filter alignment
	J2		
		A–B	Normal
		Removed	Low-pass filter alignment
	J3		
		A–B	Normal
		Removed	Defeats clamp
	J4		
		A–B	Normal
		B–C	Test ramp
	J5		
		A–B	Normal
		Removed	Defeats noise detector
	J6		
		A–B	Normal
		Removed	Defeats vertical inhibit
	J7		
		A–B	Normal mute
		Removed	Defeats video mute
4 A/D Converter Assy 1409108	No jumpers		
5 Tape H Comparator Assy 1409104	J1		
		A–B	Normal
		B–C	Test—inserts fixed error voltage
	J2		
		A–B	Normal
		B–C	Test—inserts variable dc test error voltage
6 Tape VCO Assy 1409101	J1		
		A–B	Normal
		B–C	Forces search condition
		B–D	Forces search condition
	J2		
		A–B	Normal
		B–C	Inserts test voltage for search oscillator
	J3		
		A–B	Normal
		Removed	Removes error to normal oscillator
	J4		
		A–B	Normal, remote selection of up/down oscillator
		B–C	Auto selection of up/down oscillator
	J5		
		A–B	Normal
		B–C	Test—forces VCO phase comparator
	J6		
		A–B	Single-wire heterodyne VPR-20 operation
		B–C	Two-wire heterodyne operation

Table 1-1. Test and Configuration Jumpers (Continued)

PWA	JUMPER	POSITION	FUNCTION
6 Tape VCO Assy 1409101 (Continued)	J7		
		A–B	Normal
		B–C	Test–defeats H-reset
	J8		
		A–B	Normal
		Removed	Test–verifies reset qualify counter
	J9		
		A–B	Sync head video processing Normal
	J10		
		A–B	Normal
		Removed	Disables tape vertical to vertical delay
	J11		
		A–B	Normal
		Removed	Disables VPR vertical to vertical delay
	J12		
		A–B	Back porch dropout operation
		B–C	Front porch dropout operation
7 Memory Control Assy 1409094	J1		
		A–B	Normal
		Removed	Test–disconnects overload bus
	J2		
		A–B	Normal
		Removed	Test–disables dual load
	J3		
		A–B	Normal
		Removed	Test–disconnects overload bus
	J4		
		A–B	Normal
		B–C	Test–forces slow motion
	J5		(Not used)
	J6	B–C	Used w/one-line DOC (NTSC)
		A–B	Used w/two-line DOC (1409123)
	J7		
		A–B	Normal
		Removed	Test–inhibits write address from advancing
8 S/P Converter Assy 1409122	No Jumpers		
8 S/P Converter w/DOC Assy 1409140	J1		
		A–B	Normal
		B–C	Test Data Disable
	J2	A–C	RF dropout enable (VPR-20/Het)
		A–B	TTL Dropout Enable

Table 1-1. Test and Configuration Jumpers (Continued)

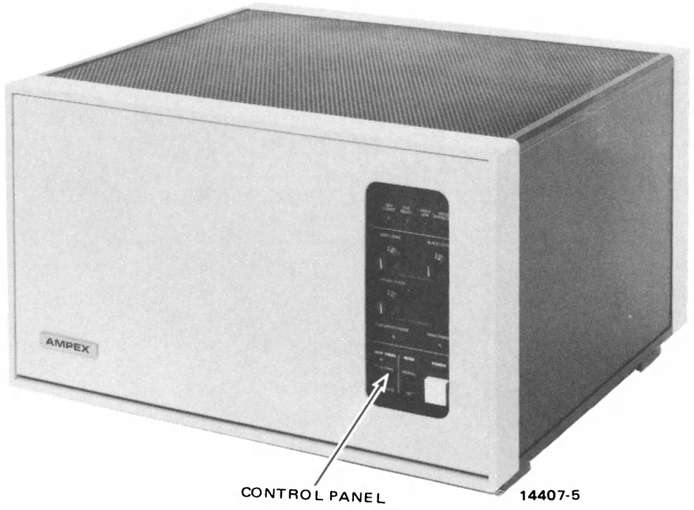
PWA	JUMPER	POSITION	FUNCTION
8 S/P Converter w/DOC Assy 1409123	J1		
		A–B	TTL Dropout Enable
		B–C	RF Dropout Enable (VPR-20/Het)
9 Memory A, B, C Assy 1409107	No Jumpers		
10	No Jumpers		
11	No Jumpers		
13 P/S Converter with Velocity Compensator Assy 1409125	J1		
		A–B	Normal
		B–C	Test—forces memory overload condition
	J2		
		A–B	Normal
		Removed	Disconnects second-order correction
	J3		
		A–B	NTSC—5-1/2 line advance
		B–C	PAL/SECAM—7-1/2 line advance
	J4		
		A–B	PAL/SECAM
		B–C	NTSC
	J5		
		A–B	Normal
		B–C	Test—inserts fixed error voltage
	J6		
		A–B	16-line memory
		B–C	12-line memory
	J7		
		A–B	PAL/SECAM
		B–C	NTSC/PAL-M
13 P/S Converter Assy 1402396	No Jumpers		
14 Video Output Assy 1405189	J1		
		RF connector	Test only—insert sweep to interpolation filter
	J2		
		A–B	Normal
		Removed	Test—removes clamp pulse
	J3		
		A–B	Normal
		Removed	Test—removes phase equalizer
	J4		
		A–B	Normal—black clip on
		Removed	Test—removes black clip

Table 1-1. Test and Configuration Jumpers (Continued)

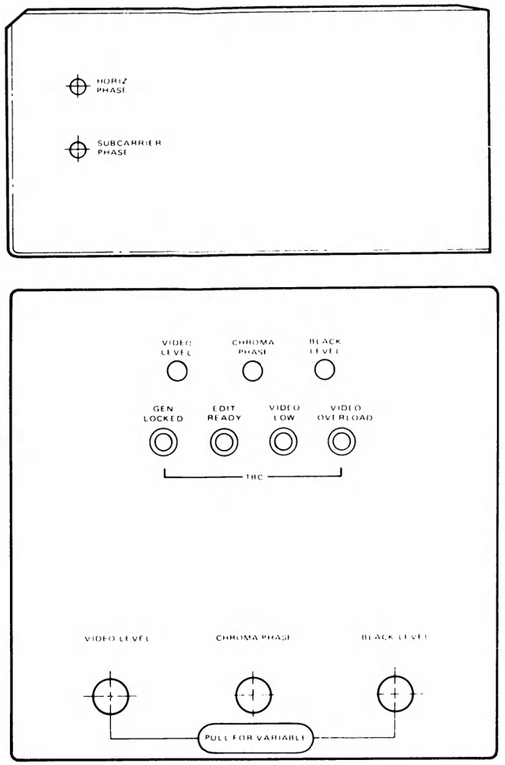
PWA	JUMPER	POSITION	FUNCTION
14 Video Output Assy 1405189 (Continued)	J5		
		A–B	Normal—composite sync on VIDEO OUT 2
		Removed	No composite sync on VIDEO OUT 2
	J6		
		A–B	Normal
		B–C	Test—inhibits V-interval clamp
15 Sync Generator Assy 1405186	J1		
		A–B	VPR-20 5-1/2 line fixed advance
		B–C	Non-servoed capstan VTR's dynamic 5-1/2 – 7-1/2 line advanced reference
	J2		Advanced reference output select
		A–B	Composite sync
		B–C	Composite sync (–8V)
		B–D	Vertical (–8V)
		B–E	Sync and burst
	J3		Reference 3.58 MHz
		A–B	
		B–C	Select jumper position as required
		B–D	for correct system operation
		B–E	
	J4		Subcarrier
		A–B	
		B–C	Select jumper position as required
		B–D	for correct system operation
		B–E	
	J5		H-phase select
		A–B	Select jumper position as required
		A–C	for correct system operation
	J6		
		A–B	RS-170 standard
		B–C	Non-standard
16 Video Processor Assy 1405146	J1		
		A–D	0° decode subcarrier
		B–C	180° decode subcarrier
	J2		
		A–B	Normal
		B–C	Test—fixed phase to decode subcarrier
	J3		
		Removed	Normal
		A–B	Test—external test generator input
	J4		
		A–B	Normal
		B–C	Test eliminates R–Y encoded chroma

Table 1-1. Test and Configuration Jumpers (Continued)

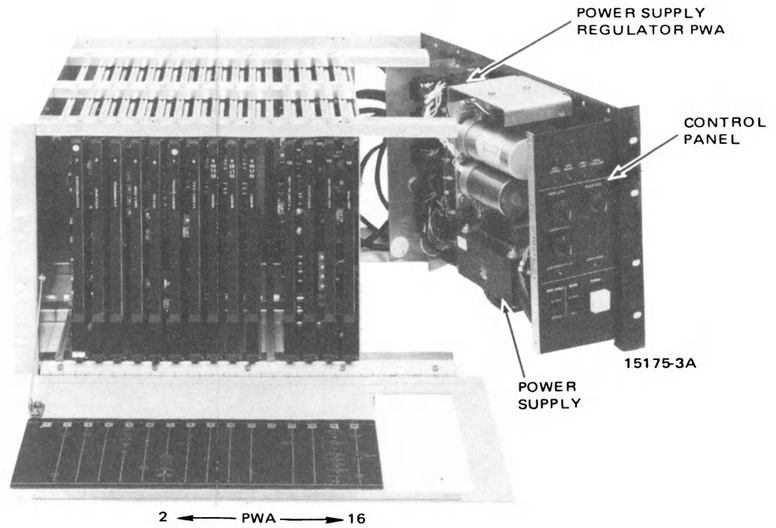
PWA	JUMPER	POSITION	FUNCTION
16 Video Processor Assy 1405146 (Continued)	J5		
		A–B	Normal
		B–C	Test—eliminates B–Y encoded chroma
	J6		
		A–B	Normal
		B–C	Test—alignment of luminance low-pass filter
	J7		
		A–B	Normal
		B–C	Test—alignment of luminance low-pass filter
	J10		
		A–B	Normal
		B–C	Test—alignment of luminance low-pass filter
	J11		
		A–B	Normal
		B–C	Test—alignment of luminance low-pass filter



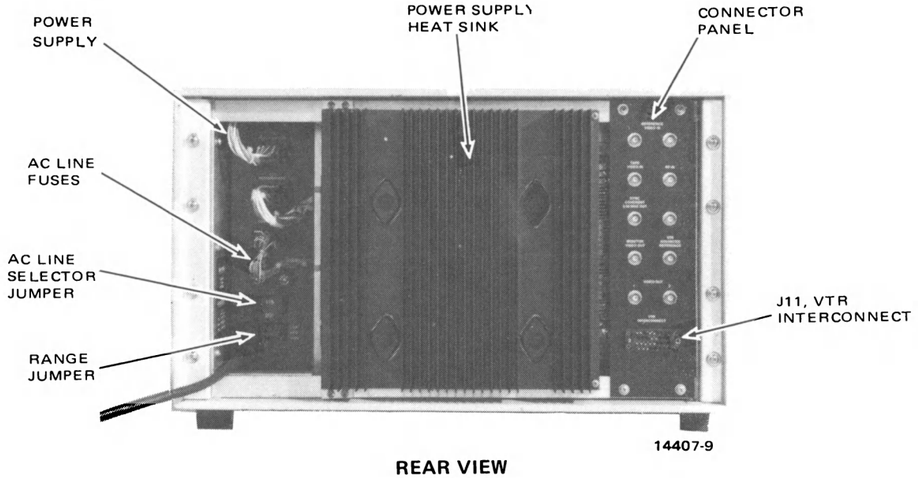
OPTIONAL STAND ALONE CABINET



REMOTE CONSOLE PANEL



BASIC TBC-2
CARD RACK (PARTIALLY
DISASSEMBLED FOR
POWER SUPPLY ACCESS)



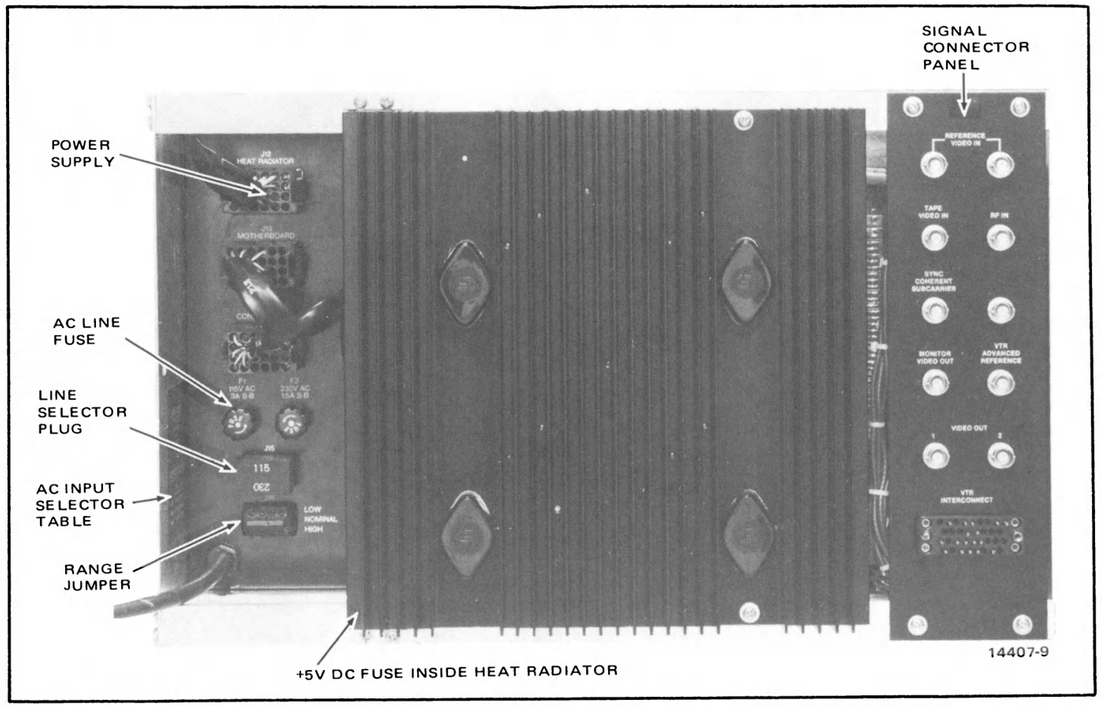
REAR VIEW

TBC BASIC ASSEMBLY	1409001
• Card Rack Assembly	1409002
Miscellaneous Parts Kit	1409153
NTSC Kit	1409133
Field Accessory Kit	1409154
Power Supply	1409155

NTSC KIT PRINTED WIRING ASSEMBLIES (PWA)		
PWA	**ASSEMBLY NO.**	**DESCRIPTION**
3	1405134	Video Input
4	1409108	Analog-to-Digital Converter
5	1409104	Tape H Comparator
6	1409101	Tape VCO
7	1409094	Memory Control
8	1409122	Serial-to-Parallel Converter
9	1409107	Memory A
10	1409107	Memory B
11	1409107	Memory C
12	—	—
13	1402396	Parallel-to-Serial Converter
14	1405189	Video Output
15	1405186	Sync Generator

TBC OPTIONS AND ACCESSORIES		
KIT	**PWA**	**KIT NO.**
Color Processor	2	1405143
Video Processor	16	1405146
Serial-to-Parallel Converter/ Dropout Compensator (One-Line)	8	1409140
Serial-to-Parallel Converter/ Dropout Compensator	8	1409123
Parallel-to-Serial Converter/ Velocity Compensator	13	1409125
Stand-Alone Rack Mount	—	1409136
Console Mount	—	1409130
Stand-Alone Cabinet	—	1409135

Figure 1-1.
System Hardware



REAR PANEL

AC POWER/RANGE JUMPER POSITIONS		
Line Voltage	**JUMPER POSITIONS**	
	Line Selector Jumper	**Range Jumper Position**
95-110	115	Low
104-126	115	Medium
114-140	115	High
190-220	230	Low
208-252	230	Medium
229-279	230	High

FUSE COMPLEMENT		
FUSE	**TYPE**	**NOTES**
AC Line		Located left rear.
115 230	3A, 125V 1.5A, 230V	Only that fuse corresponding to the AC line selection is used.
+5V Supply	Fast Blow 15A, 32V	Located inside hinged heat radiator

SIGNAL INTERCONNECTION PANEL		
	CONNECTOR	**DESCRIPTION**
	REFERENCE VIDEO IN (2)	1.0V composite video or color black (loop-thru jacks terminate in 75 ohms).
	TAPE VIDEO IN	1.0V composite video (75 ohm).
	RF IN	Dropout signal input (RF level – 0.5 to 4V, 2.5 to 10 MHz).
	SYNC COHERENT SUBCARRIER	2.0 Vp-p nominal, 3.58-MHz internally derived from tape reference, 75-ohm unterminated.
	MONITOR VIDEO OUT	1.0V composite video (75 ohm).
	VIDEO OUT 1	1.0V composite video (75 ohm).
	VIDEO OUT 2	1.0V composite or non-composite video (75 ohm).
	VTR ADVANCED REFERENCE	Advanced composite sync, 40 IRE level, nominal, sync polarity negative or advanced TTL-level composite sync or TTL-level, negative-going vertical drive.
	VTR INTERCONNECT	Used with VPR-1, -2, -2B; *VPR-20.
	pin A	Step Back
	pin B	Step Back 2
	pin C	Step Back – Signal Ground
	pin D	Step Back 2 – Signal Ground
	pin F*	Sync Retard
	pin J	Playback Vertical
	pin L	Fast Shuttle
	pin M	Playback Vertical – Signal Ground
	pin N	Edit Mute (–)
	pin P	Slow Motion
	pin R	Head Switch/Vertical Dropout
	pin S*	Zero Offset
	pin T	Head Switch/Vertical Dropout
	pin U	2H Gate
	pin V	Dropout pulse
	pin W	2H Gate – Signal Ground
	pin X*	Dropout Pulse – Signal Ground
	pin Y	Up/Down
	pin EE	Sync Head Process
	pin JJ	Step Forward
	pin NN	Step Forward – Signal Ground

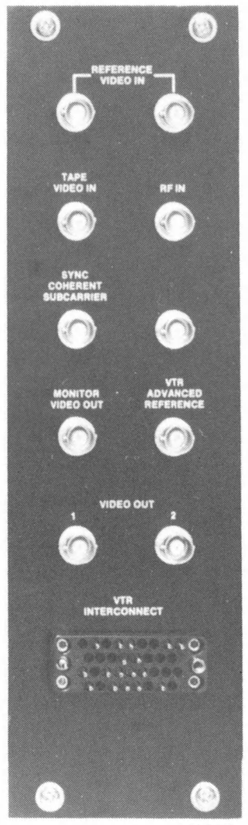
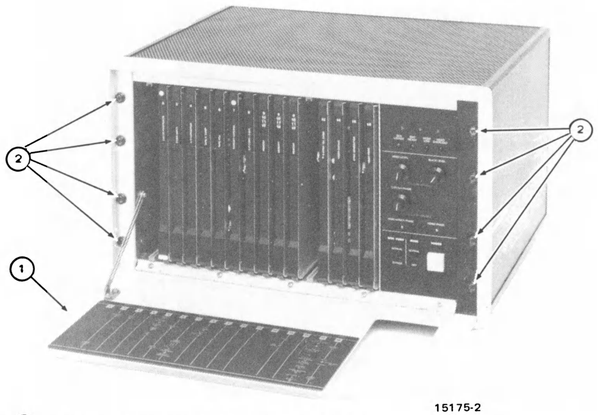
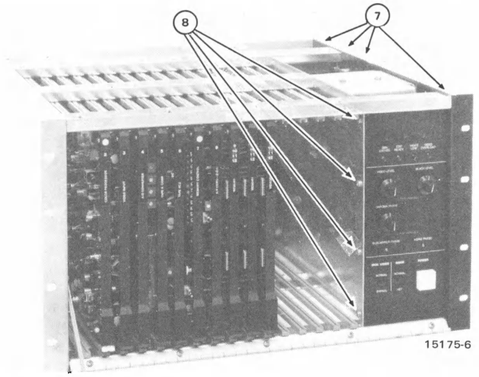


Figure 1-2.
Power and Signal Data



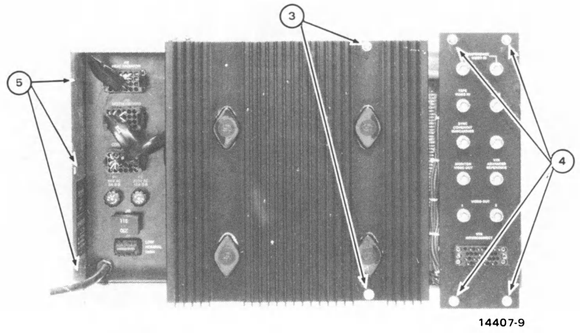
15175-2

1. OPEN MAGNETICALLY LATCHED FRONT PANEL.
2. REMOVE 4 RACK SCREWS EACH SIDE. CONSOLE VERSION ONLY: PULL THE CARD RACK FROM THE CONSOLE, PROCEED TO 7.



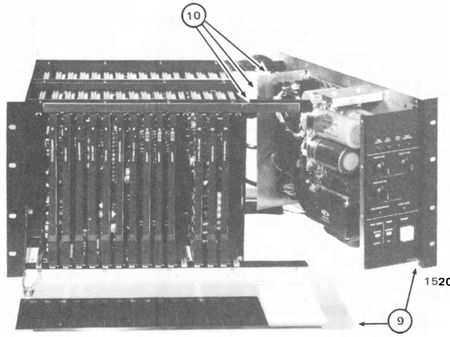
15175-6

7. REMOVE 8 SCREWS, 4 ON TOP AND 4 ON BOTTOM, (NOT VISIBLE) ON THE RIGHT SIDE OF THE CARD RACK, AND
8. REMOVE 4 SCREWS AT CONTROL PANEL LEFT FRONT



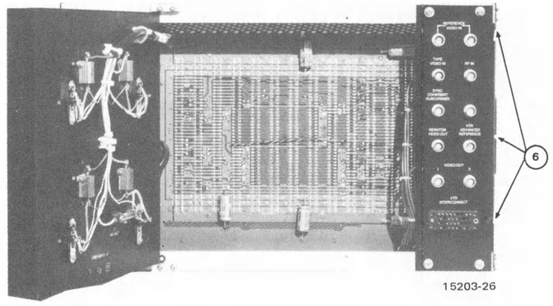
14407-9

3. LOOSEN 2 CAPTIVE SCREWS TO OPEN HINGED HEATSINK FOR ACCESS TO MOTHERBOARD.
4. REMOVE 4 SCREWS TO REMOVE CONNECTOR PANEL TO RELEASE SIDE OF CARD RACK.
5. REMOVE 3 SCREWS TO RELEASE LEFT SIDE OF CARD RACK.



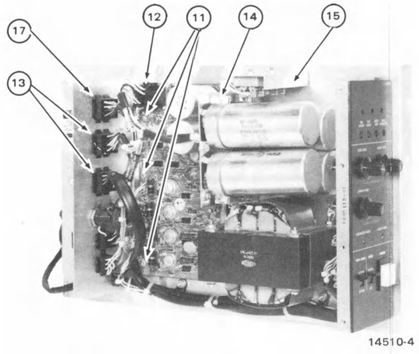
15203-27

9. SEPARATE THE CONTROL PANEL/POWER SUPPLY SECTION FOR COMPONENT ACCESS.
10. DISCONNECT 3 PLUGS (J12/J13/J14—HIDDEN) TO COMPLETELY SEPARATE ASSEMBLY FROM CARD RACK.



15203-26

6. REMOVE 3 SCREWS (NOT VISIBLE) TO RELEASE RIGHT SIDE OF CARD RACK. THE CARD RACK MAY NOW BE PULLED FROM THE FRONT OF THE CABINET.

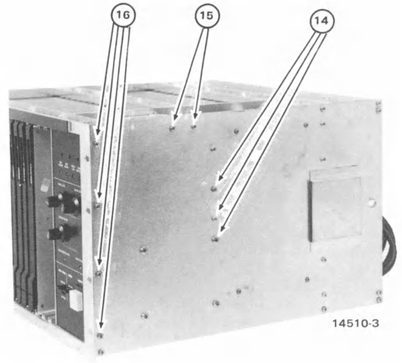


14510-4

11. REMOVE 4 CORNER AND 2 SIDE SCREWS TO LIFT REGULATOR PWA.
12. DISCONNECT PLUG J1, AND
13. RELEASE THE J12/J13 MOUNTING LATCHES TO REMOVE REGULATOR PWA AND HARNESS.
14. REMOVE 3 SCREWS ON RIGHT SIDE PANEL TO FREE CAPACITOR MOUNTING BRACKET FOR ACCESS TO CAPACITORS.
15. REMOVE 2 SCREWS ON RIGHT SIDE PANEL TO LIFT POWER SUPPLY RECTIFIER ASSEMBLY.

SELECTED COMPONENT DISASSEMBLY

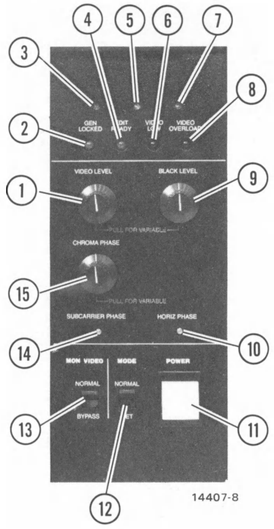
COMPONENT	MAINTENANCE ACCESS DISASSEMBLY STEPS
Card Rack—Console and Rack Mount	1 and 2
Card Rack	1 through 6
Power Supply	1 through 10
Connector Panel	4 only
Control Panel	1 through 6 plus 16 and 17
Power Supply Transistors	3 only
Power Supply Regulator	1 through 12
Power Supply Capacitors	1 through 10 plus 14
Power Supply Rectifiers	1 through 10 plus 15
+5V Supply Fuse	3 only



14510-3

16. REMOVE 4 SCREWS ON RIGHT SIDE PANEL, AND
17. RELEASE J14 MOUNTING LATCHES TO REMOVE CONTROL PANEL AND HARNESS.

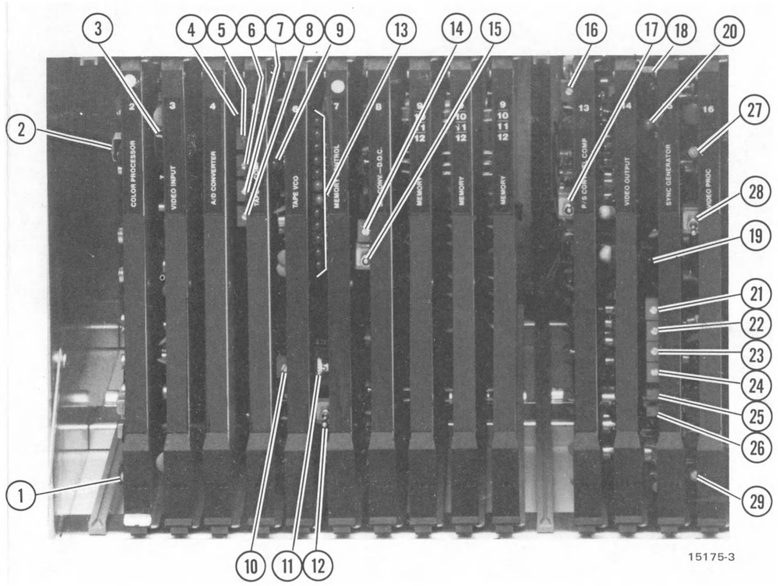
Figure 1-3. Maintenance Access Diagram

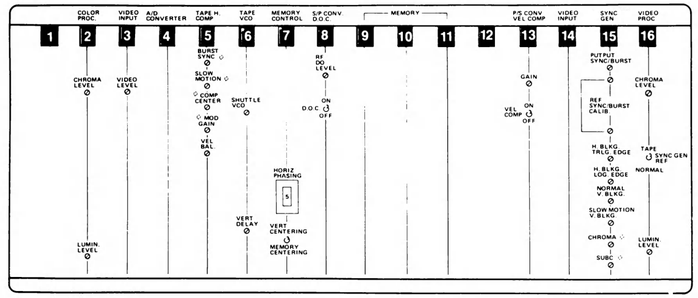


CONTROL PANEL SHOWN IS FOR THE STAND-ALONE VERSION. CONSOLE PANELS HAVE A DIFFERENT CONTROLS LAYOUT.

INDEX NO.	NAME	FUNCTION
1	VIDEO LEVEL potentiometer/switch	Adjusts the level of the video output signal. Push control "in" for unity gain.
2	GEN LOCKED indicator	Lights when the TBC-2B receives an acceptable gen lock reference signal.
3	"Unity" video level trim potentiometer	Adjusts the level of the video output signal with the VIDEO LEVEL potentiometer set to the unity gain position.
4	EDIT READY indicator	Lights when burst-to-sync phase relationship is within ±40° of RS-170A specification.

INDEX NO.	NAME	FUNCTION
5	"Unity" chroma phase trim potentiometer	Adjusts the phase of the picture chrominance information with respect to color burst during playback with the CHROMA PHASE potentiometer set to the unity gain position.
6	VIDEO LOW indicator	Lights when the video input signal level is less than 0.8 Vp-p nominal.
7	"Unity" black level trim potentiometer	Adjusts the difference between the black and blanking level of the video output signal with the BLACK LEVEL potentiometer in the unity position.
8	VIDEO OVERLOAD indicator	Lights when the video input signal level is greater than 1.25 Vp-p nominal.
9	BLACK LEVEL potentiometer/ switch	Adjusts the difference between the black and blanking levels of the video output signal. Push control "in" for unity black level.
10	HORIZ PHASE potentiometer	Adjusts H-sync phase with respect to video. Moves in increments of one subcarrier cycle.
11	POWER switch/ indicator	Turn power to the TBC on and off. Lights when switch is in the ON position.
12	MODE switch	Selects processing of heterodyne video signal when the switch is in the HET position.
13	MON VIDEO switch	Selects monitor video output signal. In NORMAL position, processed TBC video is selected. In BYPASS position, the TBC TAPE VIDEO IN is switched to the monitor.
14	SUBCARRIER PHASE potentiometer	Sets color subcarrier phase of the VIDEO OUTPUT signal with respect to an external subcarrier. Used during fully synchronous operation to match color subcarrier phase to external signal sources.
15	CHROMA PHASE potentiometer/ switch	Adjusts the phase of the picture chrominance information with respect to color burst during playback. Push control "in" for unity chroma phase.





REFER TO THE CONTROLS SUMMARY ON THE FACING PAGE FOR AN EXPLANATION OF THE PWA EDGE CONTROLS AS INDEXED HERE.

Figure 1-4. Control Panel and PWA Edge Controls (Sheet 1 of 3)

1 CHROMA LEVEL
R22 PWA2

This chroma level control is used *only* in heterodyne or slow motion and still modes. The normal mode chroma level is a function of the accuracy of the digital quantization, and response characteristics of the video signal processing circuits throughout the TBC. This control may be adjusted for the separate and different level requirements of the slow motion and heterodyne circuitry on the color processor as outlined in the PWA2 adjustment procedure.

2 LUMINANCE LEVEL
R193 PWA2

Like the chroma level, this control is used *only* in heterodyne or slow motion modes and may be adjusted differently for each mode. Refer to PWA2 adjustment section.

3 VIDEO LEVEL
R6 PWA3
VIDEO LOW/OVERLOAD Indicators

While this video level control provides a ± 2 dB range of adjustment for special cases in normal applications it should be considered the calibration control for the VIDEO LOW/VIDEO OVERLOAD indicators. The calibration point is given in the PWA3 adjustment section.

4 BURST SYNC Φ
R1 PWA5
EDIT READY Indicator

This control sets a ± 40° burst/sync phase discriminator window within which instantaneous tape error will be corrected. The calibration of this window is indicated by the Control Panel EDIT READY lamp and is calibrated at the factory to an RS 170A burst/sync phase on the odd color field. However, any off-tape burst/sync phase may be accommodated by the correction circuitry if R1 is used to turn EDIT READY on for a particular tape or section of tape. On a line-by-line basis, correction may continue even outside the ± 40° window and within a subcarrier cycle because of the compliance of the circuitry. However, step function errors such as may occur on interchange tapes with non-color-framed edits or non-standard burst/sync phase will cause a step function correction, i.e., a one-subcarrier-cycle shift of H phase. Such a correction is of consequence chiefly on matched cut edits. Bear in mind that any necessity for use of R1 is alleviated for that facility which makes RS170A tapes and uses RS170A reference throughout. Use of R1 is further amplified in "Color Framing with the VPR," Paragraph 3-16. The Standard RS170A burst/sync phase calibration may be reset through use of an RS170A standard tape or (more accurately) by the adjustment spelled out in the PWA 5 procedure for the standard window centering.

5 SLOW MOTION (burst/sync phase)
R170 PWA 5

The same burst/sync phase to which R1 burst/sync ϕ is set can also be tracked in slow motion. Any special circumstances for which R1 is adjusted to non-RS170A standard for normal speed may also force adjustment of R170 as well as R157 and R155 on PWA5. The adjustment of R170, R157, and R155 should be made in the context outlined in the PWA5 adjustment section. It should be emphasized again that this is not a recommended practice and should be reserved for the more unusual editing problems that may be encountered. The need for adjustment of R170 will be apparent if in normal play with TAPE/EE switch to TAPE and the VTR properly color framed, EDIT READY is on but goes off in the transition to or during operation in the slow or still modes.

6 Φ COMP CENTER
R2 PWA5

The standard setting for R2 is given in the PWA5 adjustment procedure, and under normal conditions it *should not* be re-adjusted. However, there are some C format tapes from VTR's with tape guide height inaccuracy which cause a larger error than the tape H qualification window on PWA 6 (Tape VCO) can tolerate as the head starts onto the tape. The result is that the TBC may select the wrong burst timing for the first three to four lines, creating a horizontal shift of one Fsc cycle. The solution for this anomaly is to shift the qualified delay (comparator timing) pulse with R2 (PWA6 TP13 —window pulse is TP12) so the pulse is adjusted for the error of the tape rather than centered in the window. Be sure to return to the standard setting for R2 as outlined in PART II, paragraph 5-7, PWA 5 adjustment.

7 Φ MOD GAIN
R3 PWA5

8 VEL BAL
R4 PWA5

16 (VEL COMP) GAIN
R1 PWA13

These three controls are optimized (the type of VTR is not a factor in the optimization) at the factory using a servo test instrument and should be adjusted only if the line error circuits on Tape H PWA5 or P/S Converter PWA 13 have been misadjusted or repaired. Use the Line Error Adjustment, Paragraph 5-8, in the Tape H PWA's procedure if adjustment becomes necessary.

9 SHUTTLE VCO Indicator

This LED indicates that the Tape VCO and Tape H circuitry are maintaining H and V synchronization for the monochrome picture during high speed shuttle of the VPR.

10 VERT DELAY
R88 PWA6

This control is used only for heterodyne VTR's or any VTR without a sync head such as the VPR-20, (Ampex VPR-1, -2, -2B machines provide their own vertical blanking dropout pulse). The setting for R88 is determined by the extent of head switching noise in the vertical interval. (Head switching noise beyond line 10 of the vertical interval may cause a step-function error which may interfere with any video information in the vertical interval.) R88 is normally set so that TBC correction begins on the second H sync pulse following the vertical. An R88 setup procedure is given in the Tape VCO PWA6 adjustment section. If the necessary setting for R88 goes beyond the second H sync pulse a readjustment to the line error circuits (R3 and R4 on PWA5 and R1 on PWA13) may be in order.

11 MEMORY LINE Centering Indicators

For standard operation the center green indicator will be on except for an occasional step function correction.

12 HORIZ PHASING
S2 PWA7

For RS170A standard off-tape video and reference, EDIT READY and the REF SYNC BURST CALIB indicator on PWA15 will be on, and S2 will normally be centered at number 5. This establishes the picture position (horizontal centering) relative to the Sync Generator H sync output. Each position of the switch moves the picture an increment of one subcarrier cycle with a two or three increment shift in either direction from the number 5 before vertical white edges (invalid data in memory) appear at either side of the screen. This control is part of the H Sync Phasing procedure, Paragraph 3-14, Part I, which should be checked if non-standard tape or reference burst/sync phase is used.

Figure 1-4. Control Panel and PWA Edge Controls Summary (Sheet 2 of 3)

13 VERT/MEMORY CENTERING S1 PWA7

The vertical centering position is for C format VPR series VTR's (or any machine with sufficiently tight servos to guarantee a nominally consistent advance that is one-half the TBC memory or 5-1/2 lines). Memory-centering is limited to non-servoed capstan heterodyne VTR's or those which do not use advanced sync. In memory centering a read/write overload (refer to the PWA7 description) may drop a line or add two lines (making the picture move up or down — a function of the loose servos and large errors common to non-servoed capstan heterodyne VTR's — whenever accumulated time-base error demands it. In vertical centering, however, playback vertical and reference vertical are compared and the correction is made.

14 RF D.O. LEVEL R24 PWA8

RF D.O. LEVEL is used only for heterodyne VTR's or those which do not supply a TTL dropout pulse (the Ampex VPR series supplies the TTL dropout pulse) and operate on the received rf level. The dropout sensitivity is adjusted by R24 and is most easily adjusted using the recommended dropout test tape listed in the Test and Maintenance Equipment table. A procedure is given in the PWA8 adjustment section for setting the dropout sensitivity when a test tape is not available.

15 DOC ON/OFF S1 PWA8

Switch S1 enables the dropout compensator option which replaces all or part of a missing line with a luminance and chroma derived from previous line(s).

16 (VEL COMP) GAIN R1 PWA13

See Numbers 7 and 8 above.

17 VEL COMP ON/OFF

Enables velocity compensator option. Refer to PWA13 adjustment section for normal vel comp operation.

18 OUTPUT SYNC/BURST R240 PWA15

This sync/burst phase control is operable *only* with PWA 15 jumper J6 in the non-RS170A B–C position. Adjustment moves the output H-sync phase relative to burst over a range of one subcarrier cycle. The control is used for matching the normal RS170A TBC output sync/burst to any non-RS170A source.

19 REF SYNC/BURST CALIB R223 PWA15 and 20 INDICATOR DS1

With RS170A reference input, R223 establishes a discriminator centering which locks the sync generator to burst zero-crossing on the odd field. This is an arbitrary calibration point which establishes the color frame sequence necessary for memory read timing (and by extension, it should be emphasized, successful color framed edits). The odd field calibration with R223 turns the REF SYNC/BURST indicator DS1 on. If the LED is not on (or has been improperly calibrated — check the *System Reference Phasing* routine in Section 3) the sync generator color frame will be ambiguous.

21 H BLKG TRLG EDGE R45 PWA15

22 H BLKG LDG EDGE R46 PWA15

The horizontal blanking leading/trailing edges are adjusted narrower than the source to prevent widening of the broadcast horizontal blanking interval. The blanking timing may be seen in the video output by turning the BLACK LEVEL control fully clockwise and observing the pedestal. The normal settings for R46 and R45 are given in the Sync Generator PWA 15 adjustment section.

23 NORMAL V BLKG R64 PWA15

24 SLOW MOTION V BLKG R65 PWA15

The normal (speed) vertical blanking may be set as far down as line 10 to unblank any V interval test and control signals, and is usually set for blanking of the line preceding such signals. Because the slow motion and still modes of operation ambiguously re-produce odd *or* even fields, the slow-motion blanking control R65 is set for blanking to end before the start of the last line prior to picture video thus blanking the ambiguous test signals which may be displaced a half line. The blanking may be seen in the video output by turning the BLACK LEVEL control fully clockwise and observing that the unblanked lines show a pedestal, blanked lines do not. See *Sync Generator Adjustment*, paragraph 15-20.

25 CHROMA Φ R146 PWA15

This Chroma Phase control like the PWA Edge Subcarrier Phase should not be adjusted with the PWA on the extender board. It is part of the basic TBC reference setup for RS170A input and will not require adjustment in any facility which uses RS170A throughout. For those facilities which use a non-RS170A reference sync/burst relationship the sync/burst calibration routine in the Sync Generator PWA15 adjustment section outlines the adjustments required to phase the TBC to that non-standard reference.

26 SUBC(arrier) Φ R208

While the control panel subcarrier phase control affects the relative phasing of both H-sync and burst, R208 subcarrier phase adjusts the output burst phase only with respect to H-sync. This control is factory-set for RS170A reference input and will not require adjustment in any facility which uses RS170A throughout. For those facilities which use a non-RS170A reference sync/burst relationship the sync/burst calibration routine in the Sync Generator PWA15 adjustment section outlines the adjustment of R208 as well as R146 (PWA edge Chroma ϕ) and other controls required to phase the TBC to that non-standard reference. R208 should not be adjusted with the PWA on the extender board.

27 SYNC GEN REF TAPE/NORMAL S1 PWA16

In the Tape position this switch enables the Video Processor PWA 16 for dubbing tapes made on non-servoed capstan VTR's. In this mode of operation off-tape vertical sync is selected by the sync generator as reference, and the off-tape video is processed for monitoring.

28 CHROMA LEVEL R35 PWA16

29 LUMIN LEVEL R181 PWA16

These chroma and luminance level controls are adjusted for standard levels to the monitor when the Video Processor is used for dubbing from non-servoed capstan VTR's. They are functional only when the Sync Gen Ref Tape/Normal switch is in the Tape position. Adjustment should be made in the context outlined in the Video Processor PWA16 adjustment section.

Figure 1-4. Control Panel and PWA Edge Controls Summary (Sheet 3 of 3)

SECTION 2

SYSTEM DESCRIPTION

2-1. INTRODUCTION

This section provides an overview of the TBC-2B Digital Time Base Corrector (NTSC) Ampex Part Number 1409000. More detail of the printed wiring assemblies (PWA's) is given in Part II of this manual where the position number of the PWA in the card rack is also the number of the tabbed sections.

2-2. SYSTEM DESCRIPTION

The TBC corrects time-base errors within a range of 10 horizontal lines to within 2.5 ns for color signals and to within 10 ns for monochrome signals. The TBC also processes still and slow-motion playback from the VPR series videotape recorders. When used with the Ampex VPR series production recorders, the TBC produces monochrome pictures at all shuttle speeds, as well as color pictures from still frame up to 10 times normal speed in either direction.

Enhanced performance of video equipment using digital techniques for switching and matched-cut editing requires exacting sync and video timing. EIA standard RS170A, illustrated in Figure 2-1, forms the basis of standard performance for the TBC. The definitions in the standard for sync/burst phase and color field are particularly relevant for an understanding of how the TBC functions. Reference throughout this manual to "standard" levels, timing, or color frame relates to the RS170A definitions of the video signal.

The TBC must lock to a particular burst/sync phase and color frame relationship by which it can accurately perform the correction. The TBC writes video picture information into memory at a rate which accurately mimics mechanical perturbations of the tape on a line-by-line basis. At the output the read function must mimic the burst/sync phase and color frame of reference video. New sync and burst are added to the picture information temporarily stored in memory and read out of memory at the reference rate.

The primary functional breakout of the TBC system is input processing, output processing, time-base error processing, and storage. Referring to the simplified block diagram in Figure 2-2, note that the memory storage consisting of PWA's 9, 10, and 11 is in the center. The input processing group is to the left and consists of the Video Input, PWA 3; the optional Color Processor, PWA 2; the A/D Converter, PWA 4; and the Serial-to-Parallel (S/P) Converter, PWA 8. The output processing group consists of the Parallel-to-Serial (P/S) Converter, PWA 13; the Video Output, PWA 14; and the optional Video Processor, PWA 16. The time-base error processing group consists of the Tape VCO, PWA 6; the Tape H Comparator, PWA 5; the Sync Generator, PWA 15; and the Memory Control, PWA 7.

For more detailed functional interrelationships among PWA's, the expanded system block diagram of Figure 2-3. A signal glossary is given in Table 2-1 which described signal functions to provide a brief overview of the system.

Table 2-1. PWA Edge Connector Signal Description

SIGNAL	FROM	TO	PURPOSE
A/D Clamp (–)	Video Input PWA 3	A/D Converter PWA 4	Triggers sync clamp in A/D input amplifier.
Advance reference	Sync Generator PWA 15	VTR	Signal to VTR to establish advance write-to-read relationship for the TBC.
Bit 1 (MSB) to Bit 8 (LSB)	A/D Converter PWA 4	Serial-to-Parallel Converter PWA 8	Digitized sample of video coded as an 8-bit binary word.
Bit 1 to Bit 24	Serial-to-Parallel Converter PWA 9	Memory PWA's 9, 10, 11	Sequence of three 8-bit binary words formatted as a 24-bit word to be stored in memory.
Black Level Control	Control Panel	Video Input PWA 3	Permits operator control of black level in the blanking interval.
Blanking	Sync Generator PWA 15	Video Output PWA 14	Vertical, horizontal blanking and mute input to composite video output driver.
Burst	Video Input PWA 3	Tape H Comparator PWA 5	Provides sync-coherent burst crossing to 6-Fsc oscillator and to burst present detector and burst crossing detector.
Burst Flag	Sync Generator PWA 15	Video Output PWA 14	Key burst flag in composite video out.
Chroma Phase	Control Panel	Sync Generator PWA 15	Operator control of reference 3.58-MHz phase.
Clamp	Tape VCO PWA 6	Color Processor PWA 2	Clamp pulse to video output amplifier.
Clamp Pulse	Sync Generator PWA 15	Video Output PWA 14	Clamp for amplitude equalizer amplifier.
Color Present	Video Input	Tape H Comparator PWA 5	Inhibits edit ready lamp in mono, operates sync select in phase error detector, replaces error voltage with fixed value.
		Tape VCO PWA 6	Input to video input switch circuit, input to selected tape VCO sync selector.
		Sync Generator PWA 15	Inhibits burst flag to Video Output PWA.
Composite Sync	Sync Generator PWA 15	Video Output PWA 14	Added to output signal.
DCϕ1, DCϕ2	Memory Control PWA 7	Serial-to-Parallel Converter PWA 8/ Dropout Compensation	Two-line memory shift clock.

Table 2-1. PWA Edge Connector Signal Description (Continued)

SIGNAL	FROM	TO	PURPOSE
Dropout Present (–)	Serial-to-Parallel Converter PWA 8	Video Input PWA 3	Inhibits one-shots during dropout.
Dual Load	Memory Control PWA 7	Memory PWA 9, 10, 11	Accesses two lines of memory to be simultaneously loaded.
Edit Mute	VPR	Memory PWA 9, 10, 11	Blank video at Video Output PWA during edit.
Encode Fsc	Tape H Comparator PWA 5	Color Processor PWA 2	Sync coherent subcarrier.
Frame/2	Memory Control PWA 7	Tape H Comparator PWA 5 Color Processor PWA 2 Parallel-to-Serial Converter PWA 13/ Dropout Compensation	Tie point. Controls phase reversal of chroma field-to-field in slow motion. PAL-M only, 12.5 Hz.
Gated Sync (–)	Video Input PWA 3	Tape VCO PWA 6	Operates sample pulse former, search 6 Fsc oscillator, enables 1.65-MHz clock.
Gen-Locked	Sync Generator PWA 15	Control Panel	Lamp indication that TBC is locked to master sync.
Head Switch Vertical Dropout	VPR	Serial-to-Parallel Converter PWA 8 Tape VCO PWA 6	VPR dropout signal during vertical blanking interval, activates dropout present generator. Generates sync head on/off signals.
Het/Normal	Control Panel	Video Input PWA 3	Inhibits 2H gate input in heterodyne.
Horizontal Phase (Coarse) Subcarrier Phase (Fine)	Control Panel	Sync Generator PWA 15	Operator control of sync-to-burst crossing phase adjustment.
Reference 7.8 kHz	Sync Generator PWA 15	Memory Control PWA 7	Helps to define odd-number fields in vertical centering operation.
RF Input	VPR	Serial-to-Parallel Converter PWA 8	Activates rf dropout signal, input to dropout present generator.
Reference Vertical (+)	Sync Generator PWA 15	Memory Control PWA 7 Video Output PWA 14	Inhibits tape 7.8 kHz to WA0, WA1 line address counters; inhibits step back from VPR for 100 microsecond delay in vertical blanking interval. Enables white bar inhibit circuit.

Table 2-1. PWA Edge Connector Signal Description (Continued)

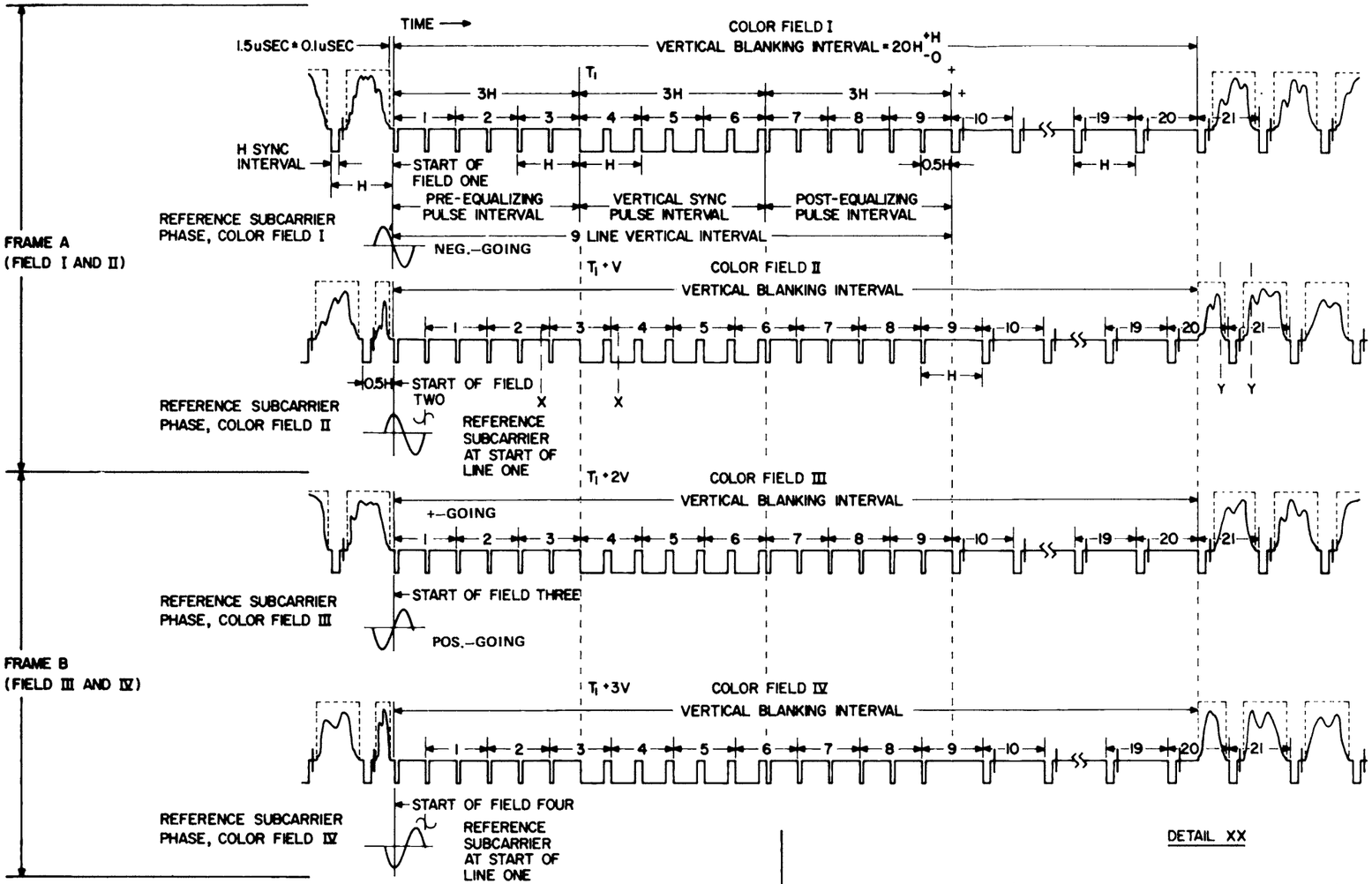
SIGNAL	FROM	TO	PURPOSE
Reference Vertical (+) (Cont.)	Sync Generator PWA 15 (Cont.)	Video Processor PWA 16	Inhibits burst sample.
Reference V/2 (+)	Sync Generator PWA 15	Memory Control PWA 7	Defines odd-number fields or color frame.
RMA, RMB, RMC	Memory Control PWA 7	Memory PWA 9, 10, 11	Memory board select, part of memory read address.
Rϕ1, Rϕ2	Memory Control PWA 7	Memory PWA 9, 10, 11	Two-phase shift register clock read function
Slow-Motion Pulse	Memory Control PWA 7	Tape VCO PWA 6	OR'ed with 1/2-line signal to correct H to burst crossing phase in slow motion.
Monitor Switch	Control Panel	Video Input PWA 3	Selects tape video or TBC video for monitor output.
Nonservo Capstan Reference Control Switch	Video Processor PWA 16	Sync Generator PWA 15	Selects LC 14.3-MHz oscillator and switches error signal to vertical comparator.
Processed Video	Color Processor PWA 2	Video Input PWA 3	Sync coherent chroma in heterodyne—alternate field phase inverted chroma in VPR slow motion.
RA0, RA1	Memory Control PWA 7	Memory PWA 9, 10, 11	Memory line select—part of memory read address.
Read Fsc	Parallel-to-Serial Converter PWA 13/Velocity Compensation	Memory Control PWA 7	Velocity compensation modulated reference Fsc from Sync Generator PWA—drives read 3 Fsc clock.
RCB1, RCB3	Memory Control PWA 7	Parallel-to-Serial Converter PWA 13	Latch and multiplexer clock.
Reference H	Sync Generator PWA 15	Video Processor PWA 16 Parallel-to-Serial Converter PWA 13/Dropout Compensation	Triggers burst sample and sync sample circuits. Triggers second order correction sample and hold.

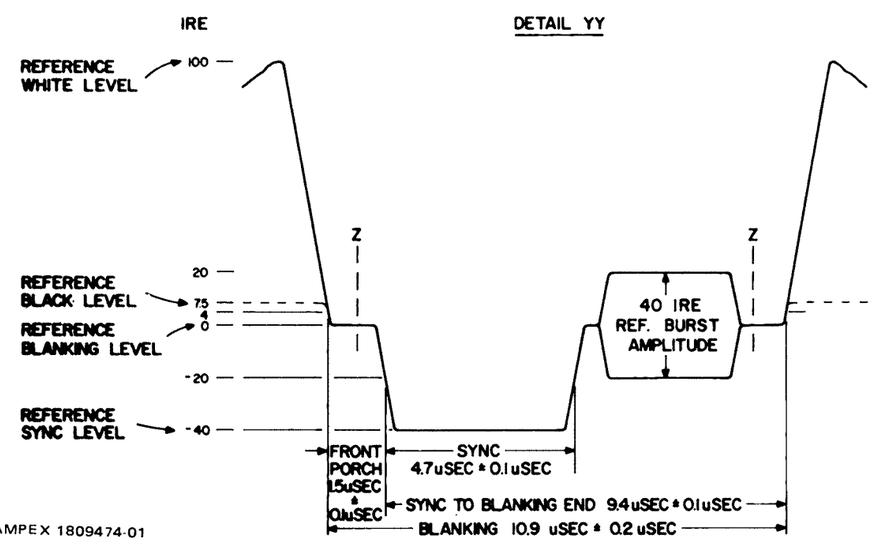
Table 2-1. PWA Edge Connector Signal Description (Continued)

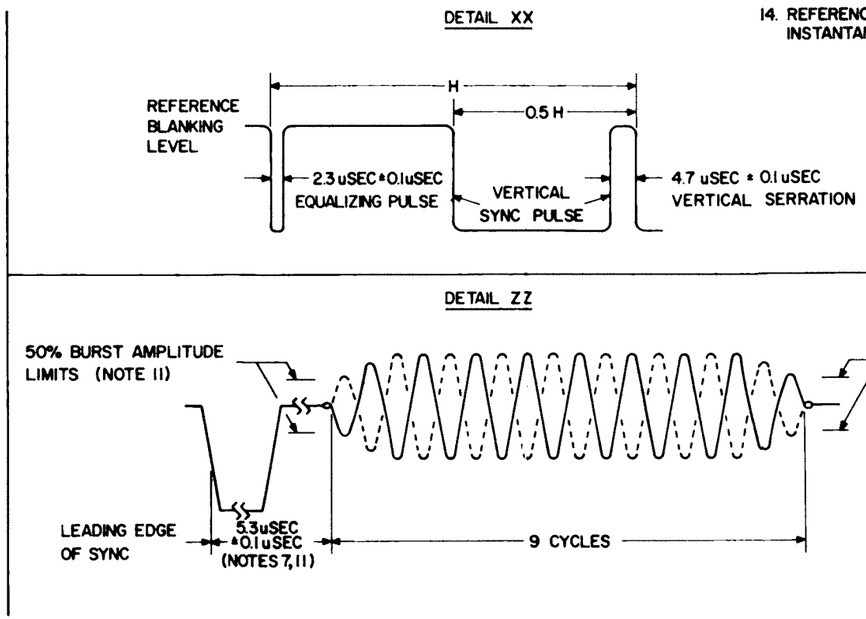
SIGNAL	FROM	TO	PURPOSE
Tape Video Input	VTR	Video Input PWA 3	Signal to be time-base corrected.
TBC Video	Video Output PWA 14 via Video Processor PWA 16	Video Input PWA 3	Provide video for studio monitor.
Terminate Write	Memory Control PWA 7	Serial-to-Parallel Converter PWA 8 Dropout Compensator	Reset two-line memory load enable.
3 Fsc	Memory Control PWA 7	A/D Converter PWA 4	Derived from tape 3 Fsc from Tape H Comparator—10.7-MHz clock for samplers and slicer latches. Clock for latches.
TTL Dropout	VPR	Serial-to-Parallel Converter PWA 8	Input to dropout present generator.
2H Gate	VPR	Video Input PWA 3	Inhibit-half-line sync pulses.
VCO Lock (–)	Tape VCO PWA 6	Video Input PWA 3	Enable noise detector during search or not qualified H (inhibits second slicer).
Vertical (+)	Tape VCO PWA 6	Video Input PWA 3	Inhibits clamp sample-and-hold during vertical blanking interval.
Vertical Inhibit (–)	Tape VCO PWA 6	Video Input PWA 3	Inhibits pulse formers of blanking and sync level sample-and-hold.
Video Input Switch	Tape VCO PWA 6	Video Input PWA 3	Selects processed video from color processor PWA 2 in heterodyne mode or VPR slow-motion (changes ramp delayed H).
Vertical Inhibit (–)	Tape VCO PWA 6	Color Processor PWA 2	Inhibits sync dc clamp pulse and burst error clamp pulse.
Video Gain	Control Panel	Video Output PWA 14	Operator control of gain of Digital-to-Analog Converter.
Video Mute	Video Input PWA 3	Video Processor PWA 16 Sync Generator PWA 15	Tie point. Locks blanking signal to kill video out.

Table 2-1. PWA Edge Connector Signal Description (Continued)

SIGNAL	FROM	TO	PURPOSE
Video Out	Video Input PWA 3	Color Processor PWA 2	In heterodyne, chroma is reencoded with sync coherent subcarrier—in slow motion, chroma is phase reversed in alternate fields.
Video Out	Video Input PWA 3	A/D Converter PWA 4	To be converted to digital data.
Video Overload (–) Video Low (–)	Video Input PWA 3	Control Panel	Drives indicator lamps—indicates abnormal video amplitude condition.
WA1, WA0	Memory Control PWA 7	Memory PWA 9, 10, 11	Memory line select—part of memory write address.
WCB1, WCB2, WCB3	Memory Control PWA 7	Serial-to-Parallel Converter PWA 8	Data latch clock.
Write Clear Reset	Memory Control PWA 7	Memory PWA 9, 10, 11	Clears memory line select register.
WMA, WMB, WMC	Memory Control PWA 7	Memory PWA 9, 10, 11	Memory board select—part of memory write address.
Zero Offset	VPR	Sync Generator PWA 15	VPR in E-E mode (direct transfer of signal).
Sync Retard	VPR	Sync Generator PWA 15	VPR control for slow motion vertical rate shift.
Mode	Control Panel	Sync Generator PWA 15	Selects normal or heterodyne mode of processing.
H Sync Phase	Control Panel	Sync Generator	Supplies analog dc control voltage.
Subcarrier	Sync Generator PWA 15	Video Output PWA 14	Output burst signal.
VCO Vertical	Sync Generator PWA 15	Tape VCO PWA 6	Servoed vertical tape pulse for non-servoed capstan mode.
Video In	Back Panel Station Reference	Sync Generator PWA 15	Composite video master reference sync in.







NOTES

1. SPECIFICATIONS APPLY TO STUDIO FACILITIES, COMMON CARRIER, STUDIO TO TRANSMITTER AND TRANSMITTER CHARACTERISTICS ARE NOT INCLUDED.
2. ALL TOLERANCES AND LIMITS SHOWN IN THIS DRAWING PERMISSIBLE ONLY FOR LONG TIME VARIATIONS.
3. THE BURST FREQUENCY SHALL BE 3.579545 MHz.
4. THE HORIZONTAL SCANNING FREQUENCY SHALL BE 2/455 TIMES THE BURST FREQUENCY.
5. THE VERTICAL SCANNING FREQUENCY SHALL BE 2/525 TIMES THE HORIZONTAL SCANNING FREQUENCY.
6. START OF COLOR FIELDS I AND III IS DEFINED BY A WHOLE LINE BETWEEN THE FIRST EQUALIZING PULSE AND THE PRECEDING H SYNC PULSE. START OF COLOR FIELDS II AND IV IS DEFINED BY A HALF LINE BETWEEN THE FIRST EQUALIZING PULSE AND THE PRECEDING H SYNC PULSE. COLOR FIELD I: THAT FIELD WITH NEGATIVE GOING ZERO-CROSSING OF REFERENCE SUBCARRIER NOMINALLY COINCIDENT WITH THE 50% AMPLITUDE POINT OF THE LEADING EDGES OF ODD NUMBERED HORIZONTAL SYNC PULSES.
7. IT IS RECOMMENDED THAT THE RELATIONSHIP BETWEEN SYNC AND REFERENCE SUBCARRIER, AS DEFINED IN NOTE 6 FOR COLOR FIELD I, BE UNIFORMLY MAINTAINED WITHIN A TOLERANCE OF ± 40° OF REFERENCE SUBCARRIER.
8. ALL RISE TIMES AND DECAY TIMES UNLESS OTHERWISE SPECIFIED ARE TO BE 0.14 uSEC ± 0.02 uSEC MEASURED FROM TEN TO NINETY PER CENT AMPLITUDE POINTS. ALL PULSE WIDTHS ARE MEASURED AT FIFTY PER CENT AMPLITUDE POINTS, UNLESS OTHERWISE SPECIFIED.
9. OVERSHOOT ON ALL PULSES DURING SYNC AND BLANKING, VERTICAL AND HORIZONTAL, SHALL NOT EXCEED TWO IRE. EXTRANEOUS SIGNALS DURING BLANKING INTERVALS, INCLUDING RESIDUAL SUBCARRIER, SHALL NOT EXCEED 2 IRE, MEASURED OVER A BANDWIDTH OF 8 MHz.
10. BURST ENVELOPE RISE TIME IS 0.30 uSEC ± 0.1uSEC MEASURED BETWEEN THE TEN AND NINETY PER CENT AMPLITUDE POINTS.
11. THE START OF BURST IS DEFINED BY THE ZERO-CROSSING (POSITIVE OR NEGATIVE SLOPE) THAT PRECEDES THE FIRST HALF CYCLE OF SUBCARRIER THAT IS 50% OR GREATER OF THE BURST AMPLITUDE.
12. THE END OF BURST IS DEFINED BY THE ZERO-CROSSING (POSITIVE OR NEGATIVE SLOPE) THAT FOLLOWS THE LAST HALF CYCLE OF SUBCARRIER THAT IS 50% OR GREATER OF THE BURST AMPLITUDE.
13. MONOCHROME SIGNALS SHALL BE IN ACCORDANCE WITH THIS DRAWING EXCEPT THAT BURST IS OMITTED, AND FIELDS III AND IV ARE IDENTICAL TO FIELDS I AND II RESPECTIVELY.
14. REFERENCE SUBCARRIER IS A CONTINUOUS SIGNAL WHICH HAS THE SAME INSTANTANEOUS PHASE AS BURST.

Figure 2-1. EIA Standard RS170A

AMPEX 1809474-01

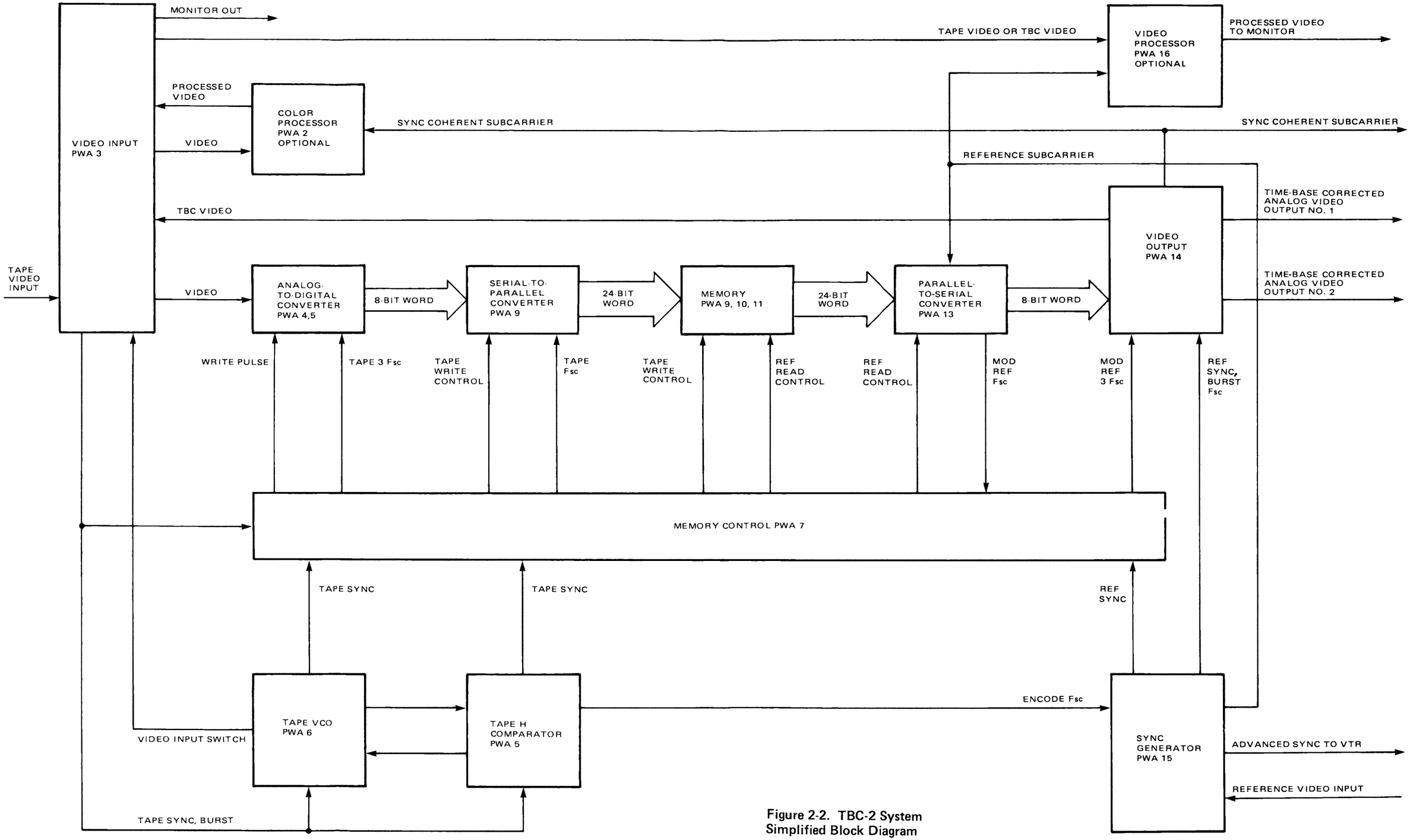


Figure 2-2. TBC-2 System Simplified Block Diagram

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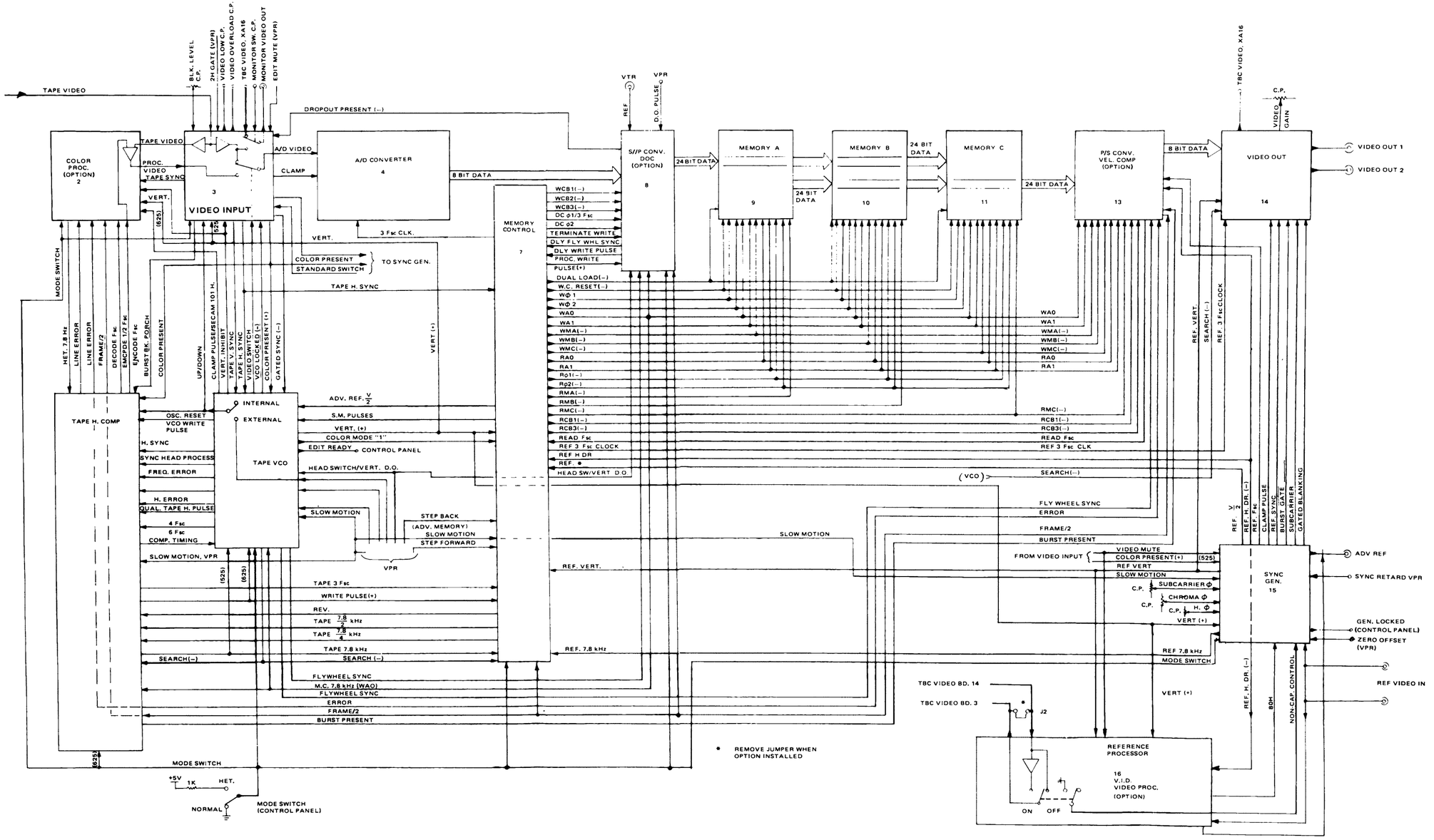


Figure 2-3. TBC (NTSC) System Block Diagram

Time-base error correction is accomplished by timing the input processing circuits synchronous to the off-tape video and timing the output processing circuits synchronous to the station reference video. The input video signal is converted to digital form by the A/D converters. The digitized video is clocked into temporary storage (Memory PWA's) by a clock whose rate is a function of the off-tape sync. The digitized video is clocked out of storage by a clock derived from the station reference signal.

The rate at which the digital video is clocked into memory follows the off-tape sync rate. Time-base nonlinearities that may have accrued during the record-play process are duplicated by the clock that stores the digital video in memory (write clock). Faster off-tape video rates result in faster rates of storage of the digital video. Slower rates result in slower storage rates. Digitized video is read out of storage at a constant rate, without time-base errors, by the read clock.(1) The read clock is generated by the crystal oscillator in the Sync Generator PWA (the read clock is produced by the Sync Generator LC oscillator during frame-lock operation with the optional Video Processor).

The color processor accessory permits the TBC to be used with the VPR series in slow-motion mode and also allows the TBC to be used with a heterodyne-type color VTR. In single-wire heterodyne mode, tape video and sync are supplied to the color processor from the Video Input PWA (see Figure 2-3). The color processor strips the non-sync-coherent chroma information from the video and demodulates it. Demodulation is effected using a chroma-coherent subcarrier derived by the Color Processor PWA from tape burst. Chroma information is added to luminance in the video after remodulation using a sync-coherent subcarrier developed by the Tape H Comparator PWA. The processed video is then routed back to the Video Input PWA which supplies it to the A/D Converter PWA. Processed video is also supplied to the MONITOR VIDEO OUT connector on the connector panel. The color processor is also used with still and slow-motion modes of operation and provides the 180° phase alternation of the chrominance information at the correct color frame phase sequence and returns the processed video to the Video Input PWA. In the normal or direct color mode, the Color Processor PWA is not required.

The off-tape video is received by the Video Input PWA, which clamps and amplifies the signal, switches the signal through the Color Processor PWA, switches off-tape or TBC video to the monitor video output, and strips color and sync information from the off-tape video signal for use by the timing circuits. The PWA also provides input video level monitoring with a video high/low warning on the control panel. In addition, the PWA contains a color/monochrome sensing circuit and a jumper-selected test ramp generator circuit that exercises the video path of the TBC for test and maintenance purposes.

The A/D Converter PWA quantizes the off-tape video into a binary digital representation of the video's instantaneous voltage level at a conversion rate of 3 Fsc (three times the 3.58-MHz subcarrier or 10.7 MHz). Each binary digital representation consists of an 8-bit data word. The Serial-to-Parallel Converter PWA combines the 8-bit data words into groups of three consecutive words and from them produces a single 24-bit word. The 24-bit word is stored in the 12-line memory at the basic clock rate of 3.57 MHz (1/3 the A/D conversion rate). Each 24-bit word defines a single cycle (279 ns) of subcarrier.

An optional one-line dropout compensator is provided on the S/P Converter PWA. The one-line dropout compensator manipulates the 8-bit data to supply replacement video which is a composite of chroma from two lines past and luminance of the previous line. Dropout compensation is accomplished by blanking the faulty video signal and recirculating the output of the compensator which corresponds to the correctly color-phased data. This replaces the current data (dropout) from the A/D converters during the time that a dropout is detected. Dropouts are identified by TTL dropout signal originating in the VPR or a loss of rf signal from the VTR.

(1) When installed, the optional velocity compensator modulates the read clock to eliminate short-term time-base errors occurring between sync pulses.

The 24-bit words from the Serial-to-Parallel Converter PWA are written into memory line-by-line synchronous to tape timing and are read out of memory line-by-line synchronous to reference timing. The 24-bit words from memory are converted back to 8-bit data words corresponding to the original video samples by the Parallel-to-Serial Converter PWA. When installed, the optional velocity compensator shares space with the Parallel-to-Serial Converter on PWA 13. Velocity errors, or short-term time-base errors that occur during each video line, produce an apparent hue shift during the line period. The velocity compensator corrects this effect by modulating the time-base of the memory read clock in the direction and by the amount that is counter to the velocity error.

In the Video Output PWA, the 8-bit words are converted back to an analog signal which, together with inserted sync burst and blanking information supplied by the Sync Generator PWA 15, provides output video from the TBC.

The memory stores 12 lines of video (four lines in each of the three Memory PWA's). When there are no time-base errors, a line of video is read out of memory six lines after it has been written into memory and memory is said to be centered. When, because of time-base errors, video is read in faster than it is read out, the read-out of a line may occur from six to 12 lines after it has been read in. Continuing high rates of writing into memory cause memory capacity to be exceeded — a condition called write over-load. Time-base errors that cause video to be read in slower than it is read out result in the read-out of a line occurring only one to five lines after it has been read in. Continuing slow writing rates cause the read memory selection circuits to try to access the same line of memory that is being accessed by the write memory selection circuits — a condition called read overload. Read or write overloads may result in picture breakup.

Ampex VPR series have a preset line-advance of off-tape video in respect to the memory read function of the TBC. The Memory Control PWA logic maintains this relationship regardless of fluctuations of tape speed. The Sync Generator PWA provides an advanced sync signal to establish the line-advance for VTR's that do not have an internal advance circuit.

Memory access signals are generated by the Memory Control PWA. This PWA also centers read-write timing of the memory after the occurrence of time-base disturbances to ensure that the buffering capability of memory is optimized. Accessing signals for the memory write process, which are generated by the Memory Control PWA, are initiated by the Tape H and Tape VCO PWA's. Accessing signals for the memory read process are initiated by the Sync Generator PWA.

The Tape H Comparator and the Tape VCO PWA's, operating together, produce the signals required by the Memory Control PWA to generate the memory write signals. Off-tape sync and burst signals, provided by the Video Input PWA, phase-lock an oscillator that develops the 3 Fsc used by the A/D Converters and the Memory Control PWA. In this way, the rate of conversion of video into digital and the loading of the data into memory are functions of tape speed. In addition, the Tape H Comparator produces a line-by-line velocity error measurement signal which it sends to the velocity compensator circuits (optional) in the Parallel-to-Serial Converter PWA. The velocity compensator stores the error and uses it to produce the modulated read Fsc signal that reduces the velocity error.

The video processor accessory enables the TBC to deliver a useful monitoring output video via the MONITOR VIDEO OUT connector when the playback is from a nonservoed capstan VTR. During this operation, the TBC is locked to the average vertical rate off-tape. The relationship of H-rate and subcarrier frequency to vertical rate is precisely determined by the TBC but since there may be appreciable error in the vertical rate of the nonservoed capstan machine, these other rates are consequently in error also. The function of the video processor accessory is to correct the subcarrier frequency so that a color monitor will

be able to lock and display stable color, even with errors in vertical rate of playback signal.

The Video Processor PWA separates chrominance from luminance, demodulates chrominance using a sync-derived 3.58 MHz, then remodulates the chrominance using a stable crystal oscillator. The chrominance is then re-added to the luminance.

For broadcastable video a further step is necessary. Off-frequency video from the main TBC output (not monitor output) must be dubbed onto a tape recorded on a servoed capstan VTR. When the resulting dub is played back locked to station reference, the TBC will process the resulting signal and deliver a broadcastable output. During this playback the TBC is locked to normal sync and subcarrier rates.

SECTION 3

SYSTEM MAINTENANCE

3-1. GENERAL

This section introduces general maintenance practices for field testing the TBC. The bulk of the adjustments should be carried out with the alignment procedures contained in the individual PWA sections of Part II of this manual. The arrangement of those sections allows a concentration of information pertinent to each PWA as a subsystem. Each section number in Part II corresponds to the numerical position of the PWA in the card rack, e.g., the Color Processor PWA 2 is Section 2 in Part II. This numbering system is used for abbreviated references in the various tables and illustrations as well as on the waveform and interconnect data in each PWA section. This also explains the absence of a Section 12 (a fourth memory position for some TBC's) and the existence of a combination Section 9/10/11 (three identical memory boards).

This system-level introduction to testing basically summarizes system adjustments in the *Installation and Operation* manual to provide a framework for adjustment or troubleshooting on a particular PWA. Summaries, checks, and adjustments in this manual guide the user in adapting the TBC to various facility requirements or returning the unit to normal operating status in the course of repair.

3-2. PREVENTIVE/ PERIODIC MAINTENANCE

Apart from keeping the unit free of dust which contributes to heat buildup, the TBC does not require preventive maintenance.

3-3. TEST EQUIPMENT REQUIREMENTS

Test equipment suggested for testing and alignment of the TBC-2B is listed in Table 3-1. Test equipment with equivalent or better specifications can be substituted for equipment suggested in the table.

3-4. SYSTEM ALIGNMENT AND TESTING

Field testing of the TBC cannot provide the kind of isolation of the individual PWA from system interactivity possible in the factory testing environment. The technician must be constantly aware of the functional relationship among PWA's when making adjustments. Indeed, there is a necessary order in which certain adjustments are made. At the system level the alignment order given in Table 3-2 should be observed to insure that a misadjustment does not take place. At the PWA level of adjustment, the order is even more exacting and adjustment (or verification of circuit parameters by checking through the procedure without actually adjusting the controls) should always proceed from the start of the procedure to the area of interest.

Alignment procedures in this section and in Part II should not be considered routine maintenance, but rather a means of returning the TBC to normal operation following repair or as a means of adapting the TBC to other VTR's or non-standard facility requirements. Results indicated in the procedures define normal operating parameters of the TBC. Fault isolation is facilitated by making checks at points described by the various procedures and by checking waveforms given for each PWA. During such checks, unnecessary adjustments should be avoided. Many of the controls are used merely to trim circuit tolerances during factory alignment and should be thought of as fixed components.

A complete alignment is not a necessary (or recommended) practice. Only that PWA in which a malfunction has occurred would likely require adjustment. The alignment order given in Table 3-2 illustrates the order a complete alignment would

Table 3-1. Test Equipment and Tools

EQUIPMENT	TYPE/FUNCTIONS
Digital Voltmeter	DC voltage accuracy to four places in the 0–20V range — HP 3465.
Oscilloscope	Dual-channel, 50-MHz bandwidth, 5 ns/div, 5 mV/div, A+B display mode, delayed sweep — Tektronix 465.
Vectorscope	Composite video and vector displays, differential gain and phase measurement, external and internal phase reference — Tektronix 520.
Signal Sources	Color bars, color black (switchable R–Y, B–Y components) variable setup level, 0–50% APL flat field, locked/unlocked subcarrier, modulated/unmodulated ramp, unmodulated stairstep — Tektronix 140 Series.
Color Video Monitor	Standard monitor for viewing stable color bars — Tektronix 650.
Dropout Test Tape	For: Ampex VPR-7500, 7800, 5800, Ampex Part No 7956027-01 Ampex VPR-7900, VPR-1, Ampex Part No. 7956028-01 Ampex VPR-1, VPR-2 Type C, Ampex Part No. 1498604-01 Ampex VPR-2B, Type C, Ampex Part No. 1498625
Extender Card	Ampex Part No. 1402453-02
Tuning Tool	AF — 12H (Mfr: Technitool)

Table 3-2. System Alignment Guide

PWA NO.	ALIGNMENT PROCEDURE	PARAGRAPH NO.
System	Power Supply	1-4
15	Sync Generator	15-9
14	Video Output	14-8
3	Video Input	3-13
6	Tape VCO	6-10/6-11
5	Tape-H Comparator (Burst Crossing)	5-7 (Steps 1, 2)
5/6/7	Tape H Sync to Video Timing	5-7 (Step 3)
5	Tape-H Comparator	5-7/5-8
7	Memory Control	7-14
2	Color Processor	2-5
4	A/D Converter	
System	Unity Gain and Controls Range	3-12 (Part I)
15	Output Subcarrier and Chroma Phasing (Repeat of Step 9 in 15-22)	15-22
5	Slow/Still/Reverse Motion	5-9

Table 3-2. System Alignment Guide (Continued)

PWA NO.	ALIGNMENT PROCEDURE	PARAGRAPH NO.
6	Shuttle	6-14
System	Color Framing with the VPR-2B	3-16 (PART I)
8	Dropout Compensator (1409140)	
	TTL	8-26
	RF Detector	6-27/8-28
8	Dropout Compensator (1409123) Delay Timing	8-30
	RF Detector	8-31
13	Velocity Compensator	13-18

take and must be used as a guide to PWA interactivity during any testing adjustments. If difficulty arises for any adjustment being done outside the order given, the technician should look for a fault or misadjustment in a preceding section. The order given here is only general, and additional notes on interactivity are provided within the various test procedures.

3-5. TAPE/REFERENCE TEST LOOP

Field testing presented in this manual uses a composite video test source for the reference video and simulated tape video as illustrated in Figure 3-1. The VTR interconnect must be used to maintain configuration integrity of the TBC as well as provide mode switching from the VTR. This method isolates the TBC from possible VTR video signal inaccuracy. VTR tape video output is required for some tests; the alternate setup is shown with broken lines.

Care must be taken to observe the proper use of loop-throughs, equal cable lengths, and terminations as illustrated.

The full instrumentation shown is not always used. Use of particular instruments is called out where required in the procedures.

This test setup replicates VPR/TBC console systems with a monitor bridge, and use of that instrumentation will be apparent throughout the procedures. It must be noted, however, that the MONITOR VIDEO OUT does not have the same accuracy as VIDEO OUT 1 and 2 for critical level measurements.

3-6. WAVEFORMS AND MEASUREMENTS

Several key waveforms are provided in the reference data for each PWA. These waveforms are referenced to the simplified schematics.

When performing adjustments given in this manual or undertaking fault analysis with the aid of waveform photos, the following should be observed:

- All pulse width measurements are made at the 50% amplitude level.
- All rise and fall times are measured from the 10 to the 90% level.
- 10:1 oscilloscope probes are used for all waveforms unless otherwise indicated.
- When taking waveforms for comparison, insure that the oscilloscope settings and triggering are as specified in the procedure or the data accompanying the waveform photo. Take special care to trigger on the odd or even field as required when using delayed sweep. The following abbreviations are used with those waveform photos which do not have CRT readouts. V for oscilloscope vertical sensitivity/cm; H for horizontal time base; UNCAL for an uncalibrated V or H setting; TRIG for oscilloscope triggering; INT for internal triggering (any external trigger source is given), and DEL for delayed sweep.

3-7. GENERAL NOTES AND PRECAUTIONS

CAUTION

ALWAYS TURN POWER OFF WHEN REMOVING OR REINSERTING PRINTED WIRING ASSEMBLIES (PWA's). FAILURE TO DO SO MAY RESULT IN DAMAGE TO THE PWA.

CAUTION

MANY ADJUSTABLE COMPONENTS HAVE BEEN SEALED WITH A SILICON COMPOUND FOLLOWING FACTORY ADJUSTMENT. TO AVOID DAMAGE TO SUCH COMPONENTS, BREAK THE SEAL BEFORE ATTEMPTING ANY ADJUSTMENT.

- Do not allow continuous overvoltage operation when adjusting the power supply. This will shorten solid-state component life.
- Use care when handling insulated gate (MOS/CMOS) field-effect semiconductor devices in order to avoid destruction or degradation of performance as a result of static charge buildup. Persons handling such devices should be grounded using a conductive wrist strap that is connected through a 1M series resistor to ground. Use great care when the humidity is 30% or less and make sure all leads of the device are shorted together (usually by the conductive material the devices are packed in) until installed into the PWA.

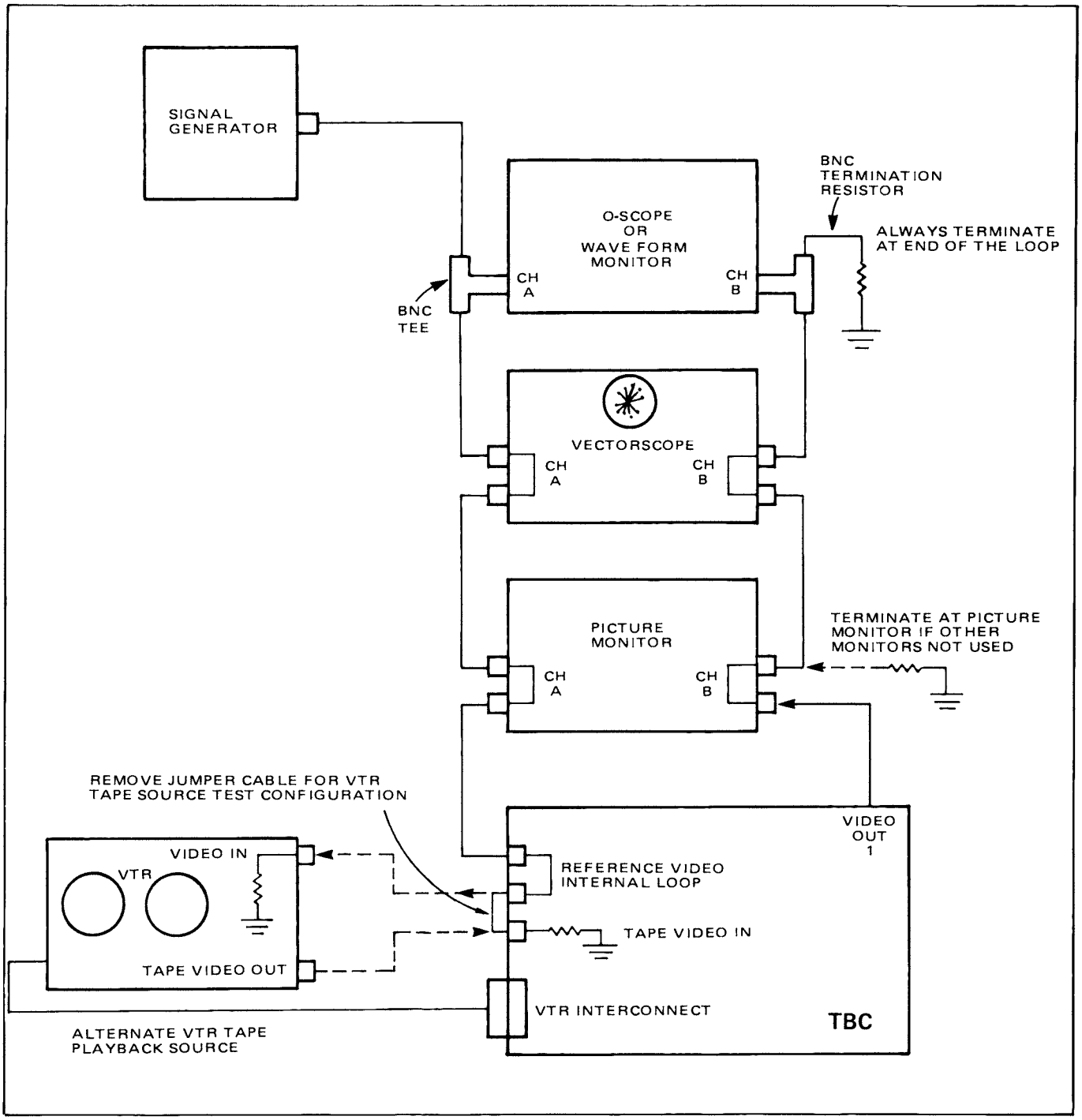


Figure 3-1. Tape/Reference Test Loop

- Adjustments and test points that are accessible at the PWA edge should be made with the PWA inserted in the card rack.

- Insure that jumpers are returned to their original positions following tests. Refer to the complete jumper list in Section 1 or the PWA jumper table in the PWA level reference data.

- Each procedure assumes that test equipment connections are removed at the completion of the procedure.

- When making adjustments or checks which do not directly involve the dropout compensator or the velocity comparator, turn them off to reduce the variables in the checks being made.

3-8. PWA EDGE CONTROLS AND INDICATORS SUMMARY

The PWA edge controls fall into two groups: those which for reasons of stability and noise interference must not be adjusted with the PWA on the extender, and those which extend the use of the TBC over a wide range of VTR, facility, and tape interchange conditions. The summary given in Section 1, Figure 1-4, describes the appropriate condition for adjustment and references the relevant adjustment procedures.

3-9. SYSTEM-LEVEL ADJUSTMENT AND OPERATION

These procedures complete the alignment of the individual PWA's at the system level and at the same time set up the TBC for normal operation in the facility. The adjustments here assume that the PWA's are aligned to the values indicated in the PWA level adjustments. If any difficulties arise with these system adjustments consult the appropriate PWA-level procedures.

3-10. System Reference Phasing Routine (with VPR-2B)

The factory setting for Reference Sync/Burst Calibration control R223 lights calibration indicator DS1 on the Sync Generator PWA 15 edge for RS170A standard reference. If DS1 is not on for a known RS170A reference input, the technique in step 1 recalibrates DS1 while illustrating aspects of color framing with which the user should be familiar. If the station reference is RS170A and DS1 is on, go to the system-phasing routine, step 2. An alternate R223 calibration procedure in the Sync Generator PWA 15 adjustment section is part of the PWA-level adjustment and furnishes a guide to adjusting sync/burst phasing to a non-RS170A facility reference where color-framed editing is not a requirement.

SETUP:

- Sync Generator PWA 15 Jumper J6 to A–B position

- Normal VPR/TBC interconnection

- 75% Color Bar, inputs to VPR and TBC reference with Standard RS170A burst/sync phase

- Scope (observe 75Ω termination requirements):

  Ch. 1: Reference video

  Ch. 2: TBC Video Out 1

  Trigger: VPR-2B PWA 14 TP7, 15 Hz frame pulse (for VPR-20 use Video PWA – TP28, Field 1 pulse)

  Vectorscope: Parallel connection with oscilloscope Channels 1 and 2. Trigger Channel 1 external subcarrier phase.

PROCEDURE:

1. *Reference Sync/Burst Phase Calibration R223).*

   a. With the setup above, play back an RS170A-recorded tape and display four vertical intervals as shown in WF1, Figure 3-2. Note that EDIT READY should be on for the RS170A-recorded tape.

b. The objective is to identify line 10 of field 3. Using the scope-delayed sweep, display a single vertical interval as shown in WF2. Note that the 1/2-line relationship between the last post-equalizing pulse and the first horizontal line with burst indicates line 10 of field 1 or 3. To further identify field 3 the sync/burst interval must be examined to find the same phase of burst between the reference and TBC output.

c. Expand delayed sweep again to display single sync/burst interval shown in WF3. Examine first cycle of burst. If bursts are of opposite phase, sync generator is producing line 10 field 1 when the reference is line 10 field 3. Field 3 is identified here with reference also to the RS170A data sheet where first cycle of burst on field 3, line 10 is negative-going and is furthermore at a nominal 5.3 μs from H sync leading edge.

d. Now turn R223 so that TBC output and reference burst phase are the same phase as shown in WF3 and DS1 is on. Center control within range of DS1 illumination. Note that there are two positions of R223 which will turn DS1 on, but only one which turns DS1 on *and* produces correct burst phase.

2. *Horizontal Phase Adjustment.* Control panel HORIZ PHASE moves the leading edge of the sync/burst interval in steps of one subcarrier cycle while control panel SUBCARRIER PHASE is a fine adjustment of burst phase within that subcarrier cycle (279 ns). Adjust HORIZ PHASE to line up leading edges within a subcarrier cycle.

3. *Subcarrier Phase Adjustment.* Using oscilloscope display for coarse phasing and the vectorscope for fine phasing adjust the control panel SUBCARRIER PHASE for same burst phase. Since reference and TBC outputs are now both RS170A, the remaining H sync phase error will be removed.

4. *Chroma Phase Adjustment.* Using vectorscope, superimpose reference and output

TOP TRACE: FACILITY REFERENCE

BOTTOM TRACE: TBC VIDEO OUT 1

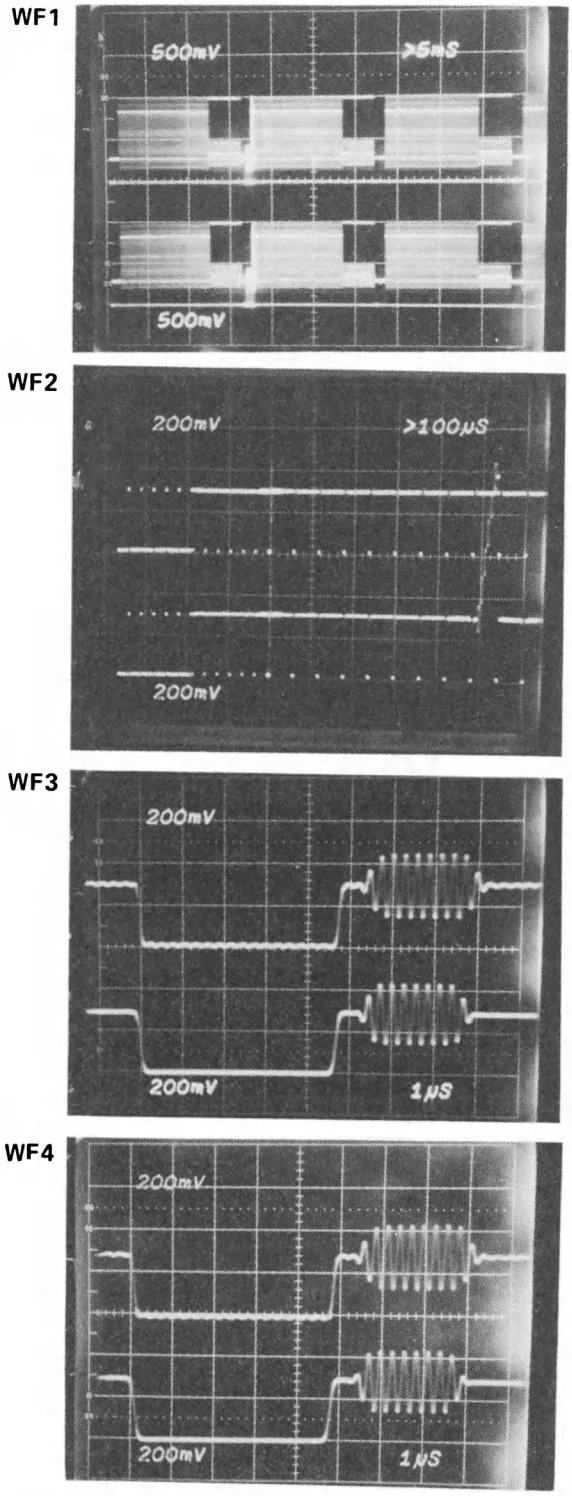


Figure 3-2. System Phasing Waveforms

chroma vectors using either variable CHROMA PHASE control or chroma phase unity trim as required.

This sync/burst calibration with R223 returns the TBC to standard RS170A setting and insures consistent color frame. If control panel controls are not appropriately centered for the operation or more subcarrier or chroma phase range is needed, a more elaborate procedure is given in the *Sync Generator PWA 15 Adjustment* (maintenance procedures) Section 15, which will return the system to the standard factory settings. That procedure may also be used to align the TBC to a non-RS170A reference where any reference sync/burst may be matched by using R208 (subcarrier phase) and R146 (chroma phase) as described in the Controls Summary, Figure 1-4, in Section 1 above.

3-11. Non-RS170A H-Sync Phasing

Output sync/burst control R240 is used to phase the output H-sync pulse to any non-RS170A equipment without affecting subcarrier phase. Reference sync/burst (R223) remains calibrated to RS170A standard reference of the facility and color frame is maintained for RS170A standard tapes but inserted H-sync from the sync generator is displayed.

1. Move Sync Generator PWA 15 jumper J6 to the B–C position and center control R240, output sync/burst.

2. Using a delayed sweep oscilloscope and vectorscope as outlined in the Standard RS170A system phasing routine, compare reference and TBC outputs.

3. Adjust the control panel HORIZ PHASE for coincidence of the sync leading edge within a subcarrier cycle.

4. Adjust the control panel SUBCARRIER PHASE to superimpose burst vectors of reference and TBC output.

5. Sync leading edge will shift as SUBCARRIER PHASE is adjusted. Adjust R240 to re-align sync leading edges.

3-12. Unity Gain and VARIABLE Controls Range

This procedure makes the final input/output adjustment of TBC unity gain which insures that with a standard VTR tape input and accurate *System Reference Phasing* the TBC will be virtually transparent. Unity trim controls for video and black levels and chroma phase can be a one-time setup adjustment for the normal or most common TBC use in the facility. These trim controls parallel the VARIABLE mode of the control function and are set for the output level/phase to be the same as that of standard input. Under standard operating conditions with the VTR operating normally, properly color framed, and tapes recorded with standard sync/burst phase, the TBC does not require adjustment. The procedure here uses the *Tape/Reference Test Loop* to illustrate unity settings in a maintenance context. The routine with a normal VTR configuration would be similar.

SETUP:

NOTE

Make certain that all inputs used during this procedure are standard 1 Vp-p levels. When comparing video input signals use cables of equal length and use 1/4% tolerance 75-ohm termination resistors into a properly calibrated oscilloscope.

- Use tape/reference test loop with a 100% color bar signal at zero percent setup level and a 100% white calibration pulse.
- Connect waveform monitor and vectorscope.
- Verify normal *System Reference Phasing* (Paragraph 3-10).
- Switch to unity (in) positions for the VIDEO LEVEL, BLACK LEVEL, and CHROMA PHASE controls.
- Switch TBC MODE to NORMAL.
- Verify following indicator conditions for normal operation:

All green indicators, on:

GEN LOCK, EDIT READY } Control Panel

REF SYNC/BURST CALIB – PWA 15

MEMORY LINE CENTER – PWA 7

Bottom green LED – Steady

Top green LED – Occasional blink

All red indicators, off:

SHUTTLE VCO – PWA 6

MEMORY OVERLOAD – PWA 7

An occasional lighting sequence here indicates a step function error correction or memory recentering due to accumulated error.

VIDEO LOW/OVERLOAD – Control Panel

There may be an occasional flash in shuttle due to unclamped video.

PROCEDURE:

1. *Video Level.* The output video level sets the gain of the final amplifier stage on Video Output PWA 14. Video LOW/OVERLOAD indications are a function of video input level to PWA 3. If a nonstandard tape is being played and either level indicator comes on, the Video Level Control R6 (PWA 3 Edge) may be used to effectively extend the range of the control panel VIDEO LEVEL. However, since R6 is the calibration control for the low/overload indicators, the PWA 3 Adjustment section should be consulted for recalibration.

   a. Adjust video level unity trim control (control panel – top left) so that peak white calibration pulse of the color bar is at 100% (100 IRE units) on waveform monitor (or a difference of less than 10 mV between input and output).

   b. Adjust VARIABLE (out) VIDEO LEVEL control fully counterclockwise. Level should be reduced to 70 (± 10) IRE units.

   c. Adjust control fully clockwise and verify a 120 (± 10) IRE unit level.

2. *Sync Levels.* Sync and burst levels should be:

   - H-sync – 286 mV (40 IRE)
   - Burst – 286 mV (40 IRE) and symmetrical with the blanking level.

   These may be adjusted at the Video Output PWA, Paragraph 14-10.

3. *Black Level.* Black level control sets up an arbitrary interval reference at the sync tip level on the A/D video on the Video Input PWA 3. This sets the range of the video to be quantized.

   a. Adjust black level unity trim control for same level between input and output.

   b. With power off remove J4 and Video Output PWA 14.

   c. Observe black reference on output color bar signal. The VARIABLE (out) BLACK LEVEL range should be 30 (± 10) IRE units.

   c. With power off return J4.

4. *Chroma Phase.* Chroma Phase Unity Trim control (control panel top-center) is set during *System Reference Phasing* routine (Paragraph 3-10). Range and centering adjustments are found in the *Sync Generation Alignment* Section at Paragraph 15-22, *Output Subcarrier and Chroma Phasing.*

3-13. Tape-H/Sync to Video Timing

These adjustments complete alignment of the write timing circuits of the Tape-H Comparator, Tape VCO, and Memory Control PWA's. Timing is set at the factory for standard RS170A burst/sync phase and will not require adjustment unless a nonstandard burst/sync phase is used or adjustments have been made to the write timing at the PWA level.

1. Use tape/reference test loop setup (Paragraph 3-5) with a 75% split field color bar signal at standard level and sync/burst phase (or the nonstandard facility reference) connected to TAPE VIDEO IN.

2. Switch TBC mode to NORMAL.

3. With power off remove Video Input PWA 3 and connect a clip lead to TP12 long enough to reach any convenient grounding point after the PWA is reinserted into the cage.

4. With power off extend Tape VCO PWA.

5. Switch power on and verify that EDIT READY and Sync Generator REFERENCE SYNC/BURST CALIBRATION indicators are on. Refer to Tape H Comparator and Sync Generator alignment procedures if indicators are not on.

6. Connect oscilloscope to VIDEO OUT 1 and using delayed sweep, line up leading edge of white bar on center graticule. Use sufficient sensitivity to see any horizontal shift within a subcarrier cycle. This will be the reference point for the next steps.

7. Ground TP12-connected clip lead and note any shift of video.

8. Adjust PWA 6 R53 (H-sync phasing) to reposition white bar edge on center graticule.

9. Alternately open and short clip lead to ground while adjusting R53 for minimum horizontal shift.

10. With power off remove clip lead from TP12 and return both PWA's to cage.

11. Turn power on and switch TBC between NORMAL and BYPASS. Note any shift in picture position.

12. If there is a shift in picture position turn thumbwheel horizontal phasing switch on Memory Control PWA to a position which minimizes horizontal shift.

NOTE

As S2 is set to its extremes a vertical line will appear at edge of screen. This is an indication that invalid data is being read out of memory, i.e., the valid data for each line of video is read out early or late as memory locations without video data are being accessed.

13. Switch TBC power on and off several times and verify that picture position remains the same.

3-14. VPR-2B Slow-Motion Operation

The VPR may be sequentially switched between normal and all slow/still/reverse speeds without picture breakup or loss of color frame. EDIT READY should remain on throughout these modes. If EDIT READY is on and properly calibrated for normal playback but goes out in slow motion a readjustment of R170 (Slow Motion Burst/Sync Phase PWA 5 Edge) may be in order. Refer to Paragraph 5-9 *Slow/Still/Reverse Motion* adjustment in Tape H Comparator adjustment section.

3-15. Shuttle Mode with the VPR-2B

The normal picture during shuttle is monochrome with black streaks. The SHUTTLE VCO indicator (PWA 6) will be on. The memory line indicators on PWA 7 will sequence randomly, and the occasional flash of the VIDEO LOW/OVERLOAD indicators on the control panel (due to unclamped video) is normal. If the picture is not stable see the PWA 6 adjustment, *Shuttle Mode Verification with the VPR-2B* (paragraph 6-13).

3-16. Color Framing with the VPR-2B

This color framing test demonstrates adjustments which affect input/output phasing and coordination with the VPR-2B controls. This in turn verifies the transparency of the TBC in terms of unity gain, system phasing, and memory write/read timing necessary for matched cut editing.

1. This test uses the normal VPR/TBC console monitor system or the VTR tape

source test configuration illustrated with the *Tape/Reference Test Loop* described in Paragraph 3-5. Complete setup as follows:

a. Loop signal generator composite video output through picture monitor channel A input then TBC REFERENCE VIDEO IN loop-through to the VPR VIDEO INPUT.

b. Connect VPR output to TBC TAPE VIDEO IN.

c. Connect TBC VIDEO OUT 1 to picture monitor channel B input (terminate).

d. Set picture SCAN switch monitor to PULSE CROSS.

e. Set INPUT MODE switch to A–B.

2. Insure that reference composite video conforms to RS170A standard (or the facility standard) for level and sync/burst phase. Use a split field 75% color bar signal.

3. Prepare for playback a known good recording of split field 75% color bars.

4. Set up TBC as follows:

a. Switch MODE to NORMAL.

b. Switch NORMAL/BYPASS to NORMAL.

c. Switch MEMORY/VERTICAL (Memory Control PWA edge) to VERTICAL.

d. Use unity positions (pushed in) for VIDEO LEVEL, BLACK LEVEL, AND CHROMA PHASE (this assumes that unity settings conform to RS170A standard video).

5. Prepare VPR-2B as follows:

a. Switch COLOR FRAMER (PWA 13 edge) and COLOR FRAME PHASE to NORMAL (usually up).

b. Switch sync head ON (Up-VPR-2B PWA 8).

6. Play back RS170A recording at normal speed and note that after a few seconds the VPR-2B SERVO light will go out indicating VPR has color framed.

7. Verify "transparency" of TBC-2B concerning sync-to-video timing relationship as follows:

NOTE

Vertical and horizontal sync of the input and output signals must be coherent, and sync-to-video timing of input and output signals must be coherent.

a. Verify that sixth (green) LED from top is illuminated on Memory Control PWA 7, that EDIT READY on control panel is on, and that REF SYNC/BURST indicator (Sync Generator PWA 15) is on.

b. Verify that display on picture monitor is completely cancelled (gray screen) and that there are no bright horizontal or vertical lines on I and Q signals.

c. If cancellation is not complete go to next step. If cancellation *is* complete, move to step 8.

d. Adjust SUBCARRIER PHASE CONTROL on TBC-2B panel for complete color cancellation.

e. On Memory Control PWA 7, adjust switch S2, HORIZONTAL PHASING, for no bright vertical lines on I and Q edges.

NOTE

If this cannot be accomplished, switch PLAY SELECT switch on the VPR-2B Color Framer PWA 13 to opposite position and then repeat step 7e.

8. Stop and start tape. The VPR should color frame (SERVO on), EDIT READY should come on, and the screen should cancel to gray. If I and Q sections do not cancel and EDIT READY does not come on, select the other position for VPR Color Framer PLAY SELECT switch. Switch VPR from

NORMAL play to SLOW and back to NORMAL to force VPR to recolor frame. EDIT READY should now be on and cancellation should be complete.

9. If necessary readjust Memory Control HORIZ PHASING switch to cancel any bright vertical lines on I and Q section edges.

10. Switch VPR from NORMAL to SLOW MOTION.

11. Verify that EDIT READY stays on. If it does not, adjust R170 (slow motion burst/sync phase-Tape H Comparator PWA 5) for EDIT READY to be on for slow, still, and reverse motion. If R170 is adjusted, re-color frame the VPR by switching between NORMAL and SLOW motion.

12. Observe picture cancellation and note that on I and Q sections a white line switches back and forth between the top and bottom of the I and Q sections. This is the normal effect of the ambiguous burst/sync phase of the repeated frame in the slow/still motion modes of the VPR.

3-17. Heterodyne Operation

Heterodyne and nonservoed capstan VTR operation requires specific jumper configurations to meet particular VTR requirements as well as a possible adjustment of advanced vertical reference, vertical blanking, and the chroma and luminance levels. This procedure reviews operation with the heterodyne and nonservoed capstan VTR's. The configuration variations for the several possible VTR's are presented here together for reference with a setup and summary procedure only part of which will be applicable to a particular VTR.

SETUP:

1. Jumper options:

PWA 15 J1	A–B	Fixed 5.5–6.5-line advance to compensate for one-half the TBC memory delay of the video.
	B–C	Dynamic Advance adjusted by R67 (advanced reference) see below.
PWA 15 J2		Advanced reference signal output options (measured at rear panel J8 — terminated)
	B–D	Vertical Sync: –4 (±0.4) V
	B–A	Composite Sync: –4 (±0.4) V
	B–E	Composite Sync/Burst: sync level 0.33 (±0.03) Vp-p, burst level 0.4 (±0.04) Vp-p.
	B–C	Composite Sync: 0.33 (±0.03) V (with VTR switched to INTERNAL SUBCARRIER)
PWA 6 J6	A–B	Sets up internal TBC sync delay processing to accommodate single-wire heterodyne and VPR-20 VTR's.
	B–C	Enables tape Fsc processing for two-wire heterodyne subcarrier input. Prevents video signal being routed through Color Processor PWA 2. Stabilization of sync-to-burst relationship is accomplished in remodulation circuits of the VTR in a two-wire operation.
PWA 8 J2 (1409140)	A–C	Enables rf dropout detector circuit.
PWA 8 J1 (1409123)	B–C	Enables rf dropout detector circuit.

2. Switches:

   a. Switch TBC MODE to HET.

   b. Memory Control PWA 7 edge: Switch VERT/MEMORY centering to MEMORY.

   c. On two-wire heterodyne VTR, switch subcarrier to external.

PROCEDURE:

With a normal TBC/VTR hookup play a standard 75% color bar recording and make any necessary adjustments as follows:

1. Advanced reference:

   a. With power off extend Sync Generator PWA 15.

   b. Connect oscilloscope

      Channel 1: Video Input PWA 3 TP1 (input video – TP1 is at PWA edge just above video level control)

      Channel 2: Sync Generator PWA 15 pin 15 (reference vertical)

      Trigger: PWA 15 pin 82 (tape vertical – use delayed sweep)

   c. Observe tape and reference vertical intervals and adjust R67 (advance reference) so that tape vertical sync leads reference by 5.5 lines.

   d. With power off return sync generator to the cage.

2. Chroma and luminance levels:

   No adjustment should be required for a standard level tape. If adjustment is necessary, follow procedure outlined in *Color Processor* adjustments, Paragraph 2-7, using a normal tape input. Note that levels should be reset for VPR slow motion operation.

3. Vertical delay:

   Some VTR's may require readjustment of the vertical delay circuit on the Tape VCO PWA 6 to eliminate head switching transients in vertical interval. Consult Paragraph 6-12 in the tape VCO adjustment section.

4. Dropout compensator rf detector:

   Consult the appropriate adjustment procedure (Paragraph 8-25 for Assembly 1409140 or Paragraph 8-29 for Assembly 1409123) in the S/P Converter PWA 8 maintenance section to adjust the dropout level with or without a dropout test tape.

3-18. VPR-20 Operation

The C format VPR-20 operation uses the same Tape VCO jumper configurations as the VPR-2B with sync head, but unlike the VPR-2B an advanced reference must be used because the VPR-20 does not have internal circuitry to compensate for the TBC memory delay (one-half the 12-line memory).

SETUP:

1. Jumpers:

   The following jumper positions must be used:

PWA 6 J6	A–B	Sets up normal internal TBC sync delay.
J9	A–B	For sync head video processing.
J12	A–B	For back porch format dropout operation.
J4	B–C	For internal control of the VCO search oscillators.
PWA 8 J2 (1409140)	A–C	Enables rf dropout detector circuit.
PWA 8 J1	B–C	Enables rf dropout detector circuit.
PWA 15 J1	A–B	Fixed, 5.5-line advance to compensate for one-half the TBC memory delay of the video.
J2	B–E	Selects composite sync with burst advanced reference signal out for VPR-20 servo.

2. Switches:

   a. Select Memory Control PWA 8 MEMORY centering.

b. If Video Input PWA 3 has VPR-20 interface kit (1460189) set switch on (up). An initial setup for the VPR-20 interface kit is given in the *Video Input Adjustment* section, Paragraph 3-16.

PROCEDURE:

There are no adjustments to be made separately for VPR-20 operation that are not common to the basic TBC adjustments given in this manual for normal VPR-2B operation except for the VPR-20 interface kit mentioned above.

The VPR-20 playback will give the same control panel and PWA Edge Control indications outlined for the VPR-2B in Paragraph 3-12, *Unity Gain.*

3-19. FAULT ISOLATION

The first step in fault isolation is to reduce variables by setting up the tape/reference test loop and turning off the dropout and velocity compensators. Then, making certain the input tape and reference video are standard, begin checking for normal conditions following the pattern of *System Alignment* order (Paragraph 3-4).

3-20. Reference Data

The arrangement of this manual puts theory description and maintenance information in a single section for each PWA in order to enhance the potential for informed testing. A series of reference data sheets at the end of each section supports both the descriptive and maintenance information. These data sheets contain key waveforms as well as summaries of test points, controls, and jumpers. Simplified schematics give one-shot times, counter pre-loads, and interconnect data. See Section 1 of Part II to become familiar with the arrangement and use of the reference data.

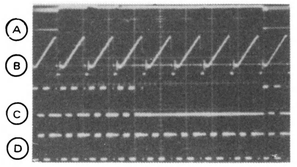
3-21. Digital Path Faults

Interestingly, digital path faults are easier to recognize than some of the analog and timing subtleties of the TBC. The Test Ramp Bit Finder diagram, Figure 3-3, reveals some typical faults. The diagram is entirely self-explanatory and assumes that the dropout compensator is switched off. Sample comparison waveforms of specific missing bits and the accompanying notes provide a method of identifying faulty devices at various points in the digital path.

SET UP CONDITIONS

- COLOR BARS TO TAPE VIDEO IN AND REFERENCE VIDEO IN
- JUMPER J4 (PWA 3) TO B–C
- SWITCH A7-S1 TO DROPOUT COMP (DOC) OFF
- SWITCH A10-S1 TO VEL COMP OFF
- OSCILLOSCOPE CH. A TO A9U14-4
- OSCILLOSCOPE CH. B TO VIDEO OUT 1
- TRIGGER OSCILLOSCOPE ON Wϕ1: A7 PIN 18
- SETUP SHOWS 8 LINES AS IN WAVEFORM 1. CHANNEL C AND D SHOW THE MEMORY LINE AND BIT OF INTEREST.

WF1



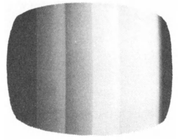
(A) A9-U14 (R1ϕ1 READ CLOCK). LINE 1 REFERENCE

(B) VIDEO OUT 1 SHOWING 8 LINES

(C) A9-U15-8, BIT 10 (BIT 2 OF 10.7 MHz BYTE 2 SHOWING MEMORY OUTPUT OF BIT 10 FOR LINES 1 THROUGH 4. NOTE THAT THERE IS NO OUTPUT FROM U15-8 DURING LINES 5-8

(D) A9 PIN 42, BIT 10 SHOWN FOR LINES 1-8 ON THE COMMON MEMORY BUS

DIGITAL PATH FAULT SYMPTOM

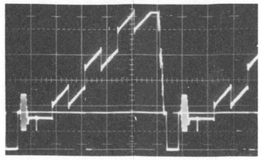


TWO OR MORE VERTICAL BARS IN THE MONITOR VIDEO INDICATE A FAULT IN THE DIGITAL PATH.

THE DISPLAY SHOWN IS THE RESULT OF GROUNDING A9 PIN 79 (BIT 3 OF THE 24 BIT BYTE, A 3.58 MHz RATE FAULT)

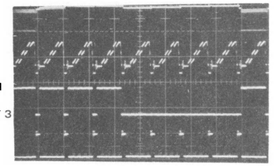
10.7 MHz RATE FAULT

WF2



A FAULT IN ONE OF THE 10.7 MHz RATE 8 BITS (A/D AND THE DATA SECTION OF THE S/P AND P/S CONVERTERS) APPEARS AS STEPS IN THE VIDEO OUTPUT (WF2 ABOVE), THE RESULT OF GROUNDING A8-PIN 42, AT INPUT TO S/P CONVERTER.

WF3



(A) A9-U14-4

(B) VIDEO OUT 1

(C) A9-U15 2/BIT 3

(D) A9-PIN 35

WITH BIT 3 LOW AT THE S/P CONV, INPUT, PIN 42. NOTE IN WF3 THAT THE STEPS APPEAR IN ALL 8 LINES (TRACE (B)). TRACE (D) IN WF3 SHOWS THE LOW OUTPUT FOR BIT 3 (OF THE SERIAL 8 BIT BYTE). PINS 43 AND 51 (BIT 3 OF THE SECOND AND THIRD SERIAL 8 BITS) ARE SIMILARLY LOW.

A MISSING 1 OF 8 BIT IS EASILY IDENTIFIED BY MISSING BITS AT THE 3 CORRESPONDING BIT LOCATIONS EVERYWHERE IN THE 3.58 MHz RATE PARALLEL 24 BIT PATH.

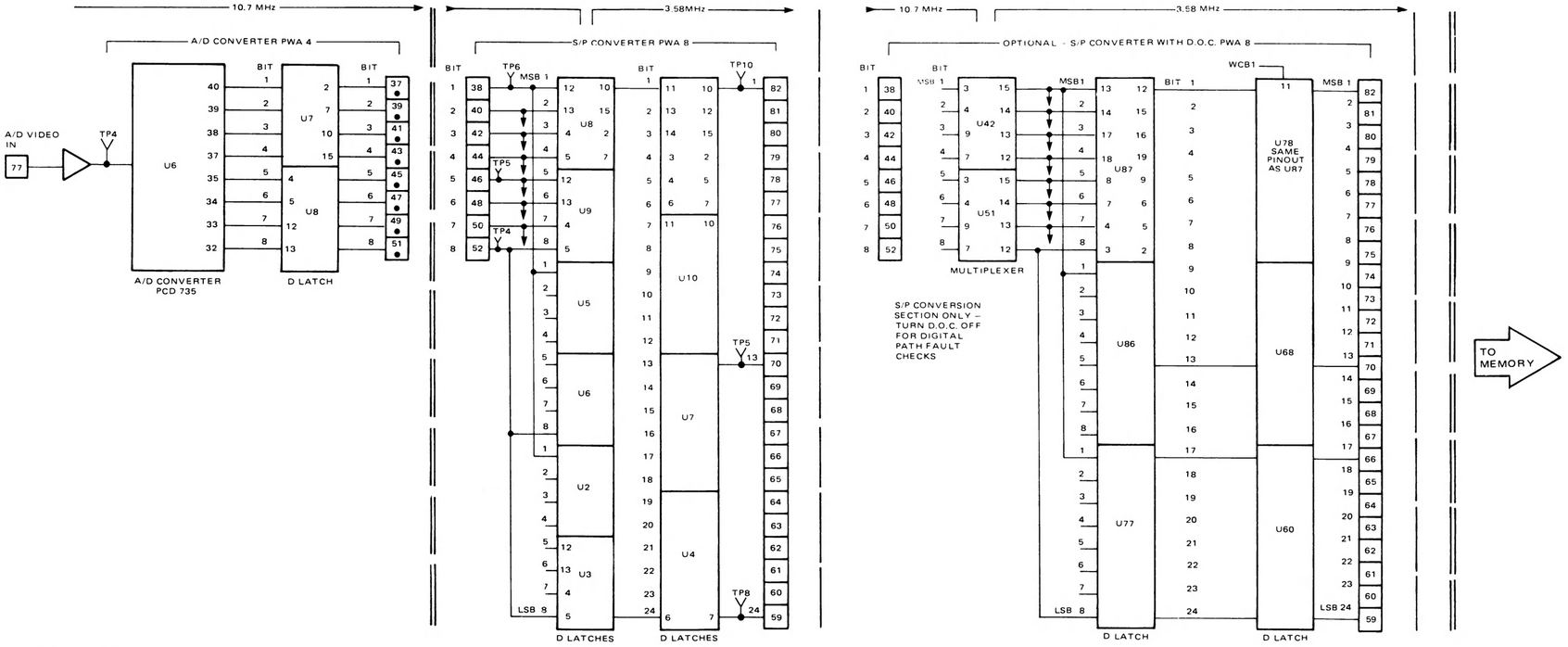
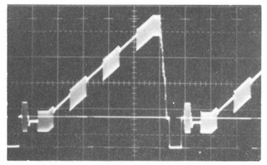


Figure 3-3. Digital Path Interconnection/ Test Ramp Bit Finder Diagram (Sheet 1 of 2)

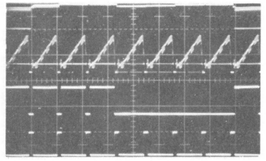
WF4



A FAULT IN ONE OF THE 3.58-MHz RATE 24 BITS (MEMORY AND THE PARALLEL SECTION OF THE S/P AND P/S CONVERTERS APPEARS AS BURST RATE NOISE ON THE RAMP AT THE VIDEO OUTPUT SHOWN IN WF4 ABOVE. THE RESULT OF GROUNDING A8-PIN 80 (BIT 3 OF 24).

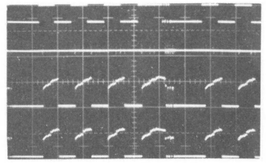
WF5

- (A) A9-U14-4
- (B) VIDEO OUT 1
- (C) U15-2 BIT 1 (A9)
- (D) A9-PIN 35



WF6

- (A) A8-PIN 42
- (B) A8-PIN 80
- (C) A8-PIN 72
- (D) A8-PIN 64

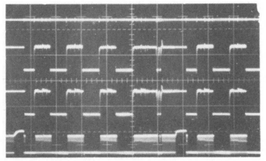


THE BURST RATE NOISE IS SEEN ON ALL EIGHT LINES AT TRACE (B) OF WF5. THE MISSING BIT 3 IS SHOWN IN TRACE (D) IN WF5, MEMORY OUTPUT, AND IN TRACE (B) IN WF6 (NOTE ALSO THAT TRACE (A) IN WF6 IS THE 10.7 MHz RATE BIT 3 INPUT TO THE S/P CONVERTER, AND TRACES (B), (C), AND (D) ARE THE PARALLEL OUTPUTS FOR BIT 3 BITS 3, 11, AND 19). BIT 3 IS ALSO LOW AT THE A13 INPUT IN TRACE (A) OF WF7, WHILE BIT 11, TRACE (B), AND BIT 19, TRACE (C) ARE NORMAL. COMPARE THE ABNORMAL TRACE (D) WITH WF 8, FIGURE 2-28.

WF8 AT RIGHT SHOWS TYPICAL CONDITIONS FOR A BAD MEMORY IC. NOTE THAT ONLY LINE 5 HAS THE BURST NOISE IN THE RAMP. LINE 5 IS ON MEMORY PWA A10–LINE 1. IN THIS CASE, U23-10 FAILED.

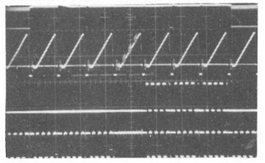
WF7

- (A) A13-PIN 36
- (B) A13-PIN 44
- (C) A13 PIN-52
- (D) A13-PIN 20



WF8

- (A) A9-U14-4
- (B) VIDEO OUT 1
- (C) A10-U15-2
- (D) A10-PIN 35



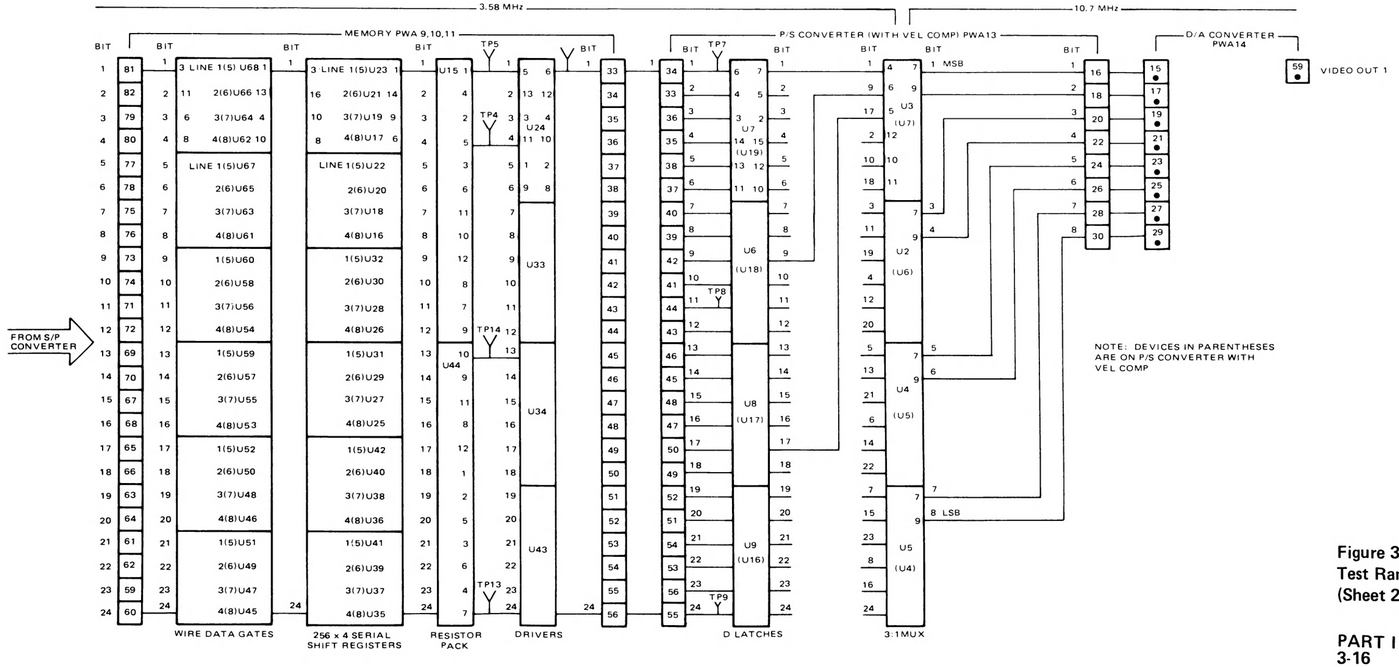


Figure 3-3. Digital Path Interconnection/ Test Ramp Bit Finder Diagram (Sheet 2 of 2)

PART II

PWA-LEVEL

DESCRIPTION AND MAINTENANCE

SECTIONS 1 THROUGH 16

SECTION 1

PWA-LEVEL

DESCRIPTION AND MAINTENANCE

1-1. INTRODUCTION

In this part of the manual, each of the printed wiring subassemblies (PWA's) is presented in a separate section. The section number corresponds to the numerical position of the PWA in the card rack. Thus, the Video Input PWA 3 is at slot 3 of the rack. In tables and illustrations, references to the printed wiring assemblies are often abbreviated to their PWA numbers for quick indexing among sections. The power supply does not have an assembly number and is presented in this section.

Each PWA section has the same three-part organization:

- *DESCRIPTION*
- *MAINTENANCE*
- *REFERENCE DATA*

Reference data serves both the description and maintenance texts and consists of a series of foldouts containing block diagrams, simplified schematics, timing and test waveforms, and other maintenance data. These are indexed in the introduction to each section. The introduction also contains a summary of the major functions of the PWA for quick reference.

1-2. PWA-LEVEL DESCRIPTION

Theory consists of a general description of the functions of the PWA at the block level. Block diagrams, simplified schematics, and timing waveforms in the reference data section supplement this discussion with additional circuit detail as well as system interconnect information to aid in following functional details not directly addressed in the text. The maintenance procedure should also be studied to round out circuit details for a fuller understanding of the TBC system.

1-3. PWA-LEVEL MAINTENANCE

Maintenance protocol for the TBC is outlined in the *System Maintenance* section of Part I. That section should be reviewed before undertaking any adjustments. Observing the *System Alignment Guide,* Table 3-2, is crucial to making accurate and reliable adjustment. To reduce variables in field testing, the TBC is partly isolated from the VPR using the *Tape/Reference Test Loop* described in Paragraph 3-5 (Part I).

Maintenance procedures are aimed at: (1) reestablishing factory-set parameters following repair or misadjustment, (2) providing the proper context for adjustment of certain controls for unique VTR or facility requirements and (3) providing key data points for fault isolation.

Adjustments should not be made outside the context of a given procedure. Some controls (chiefly filters) are factory-only adjustments. These will be noted in the adjustable controls summaries in the reference section for each PWA. Failure to meet adjustment parameters at any point in the PWA-level procedures may indicate a fault or misadjustment of a prerequisite interactive function. Annotated schematics provide an easy means of tracing an interactive series of adjustments through the system with the use of the interconnect data. Waveforms may also be consulted for normal TBC operation.

1-4. REFERENCE DATA SHEETS

Reference data at the end of each section supports both the description and maintenance texts.

The arrangement and type of data is the same for each PWA and consists of the following:

- **Overall Block Diagram** The block diagram provides a functional layout and component designators referenced to the schematics.
- **Simplified Schematics** These schematics may be used for a study of the system and for fault analysis, but final proof of faults should rest on the documents in the *Parts Lists and Schematics* manual. In addition to waveform call-outs, these schematics provide calculated one-shot times, counter pre-loading, and occasional notes on circuit operation. The interconnect data provides a guide to system interactivity.
- **Waveforms** Waveform references in the description and maintenance texts use an alpha-numeric designator such as WF12/WF13 (H). This indexing accommodates the repetition of certain waveform test points for several operational and timing modes. As timing diagrams, waveforms provide a record of normal operation with a VPR-2B.
- **Maintenance Data** Maintenance data is always the last reference sheet in the section (except for PWA 8 and PWA 13 which are multiple options). Each data sheet contains test points, adjustable controls, and jumper summaries as well as a component locator diagram to locate devices called out in the maintenance procedures. The adjustable controls summary should be consulted as a reference to factory-only adjustments.

1-5. POWER SUPPLY

Refer to the following documents in the *Parts Lists and Schematics* manual:

ASSEMBLY No. 1409155

SCHEMATIC No. 1409157

Refer to the following reference data sheets:

Detailed Block Diagram – REFERENCE 1

Test/Maintenance Data – REFERENCE 2

1-6. Power Supply Description

The power supply transformer/regulator assembly is mounted behind the control panel; the output load transistors are mounted on the rear hinged heat sink panel which also carries the 5-Vdc supply fuse. The mechanical configuration can be seen in the maintenance access diagram, Figure 1-4 in the Part I *System Hardware* section. A detailed block diagram with interconnections is given in REFERENCE 1 at the end of this section.

1-7. Power Supply Check

NOTE

The power supply does not require routine adjustment and should not be adjusted unless the need is well established. Power supply output voltages should be checked under typical line voltages and load conditions.

Fuse requirements (and location) and normal output voltages are given in REFERENCE 2 at the end of this section.

Check output voltages as follows:

1. Insert PWA extender board into position number 1 of card rack.
2. Check voltages at test points given in *Power Supply Output Limits* table in REFERENCE 2 at the end of this section.

NOTE

If all voltages measured in prior steps are within given tolerances, do not proceed to the adjustment. Even with out-of-tolerance voltage readings, reasonable assurance that an overload is not causing the condition should be obtained before attempting voltage adjustment. A misadjusted power supply can cause all PWA adjustments to be out of tolerance.

1-8. Power Supply Adjustment

1. Referring to the maintenance access diagram, Figure 1-3 in the Part I *System Hardware*

section, pull card cage from cabinet. Two controls will be seen at the top of the regulator PWA. Refer to the component locator in REFERENCE 2 for the test point locations.

2. At voltage regulator assembly, connect digital voltmeter between TP8 (REF +12V) and TP6 (REF GND).

CAUTION

EXERCISE CARE WHEN MAKING ADJUSTMENTS. CONTINUOUS OVERVOLTAGE OPERATION OF SOLID-STATE COMPONENTS CAN SHORTEN THEIR LIFE.

3. Turn power on and adjust R85 (+12V ADJ) for +12.000V.

NOTE

The +12V must be adjusted before the -12V.

4. Connect digital voltmeter between TP7 (REF -12V) and TP6 (REF GND).

5. Adjust R85 (-12 ADJ) for -12.000V.

6. Using digital voltmeter, verify the following voltages between TP6 (REF GND) and specified test points:

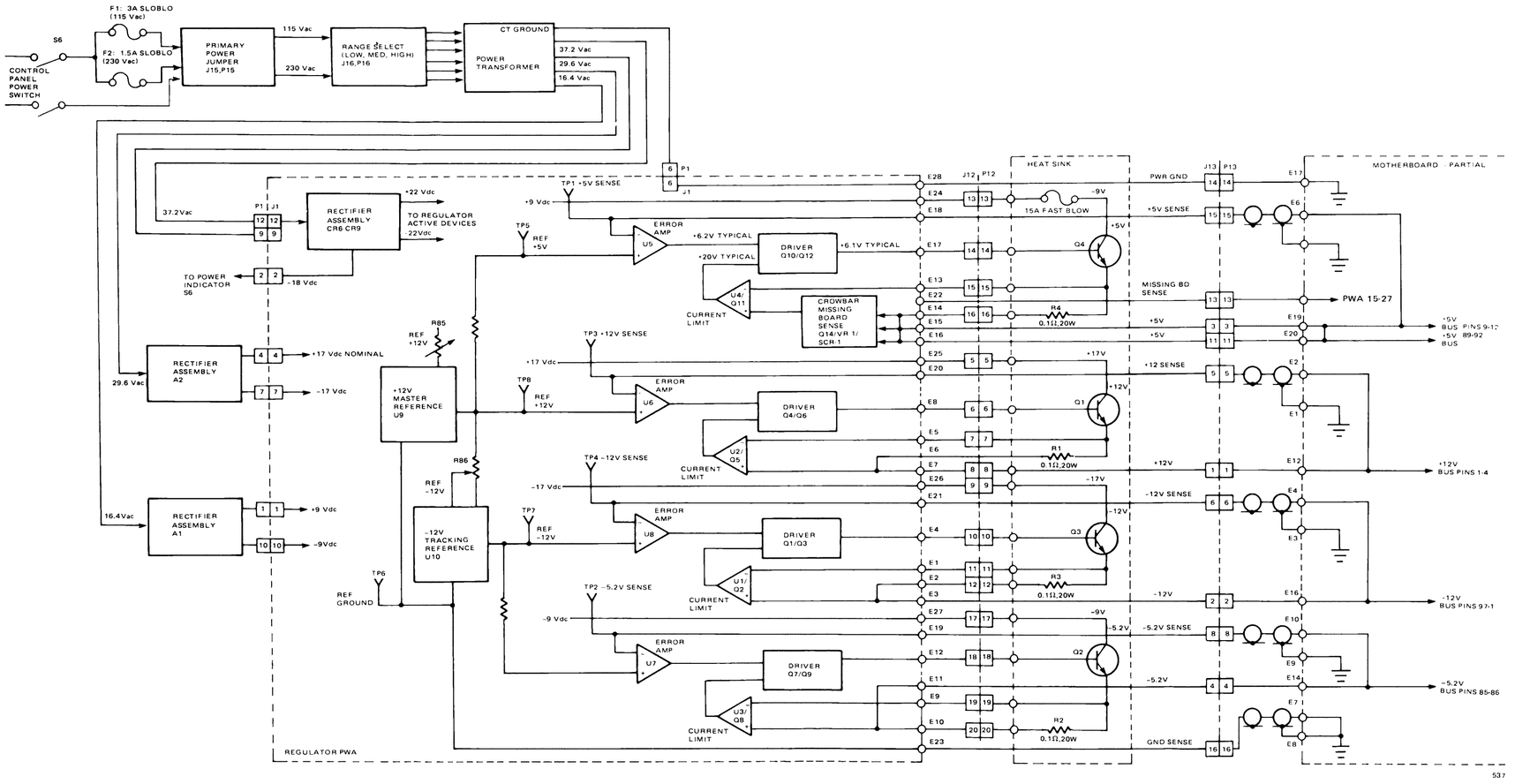
   a. TP1: +5.000 (± 0.050)V

   b. TP2: -5.200 (± 0.010)V

   c. TP3: +12.000 (± 0.100)V

   d. TP4: -12.000 (± 0.010)V

7. Switch power off and return card rack to cabinet.



Power Supply Block Diagram
REFERENCE 1

Fuses

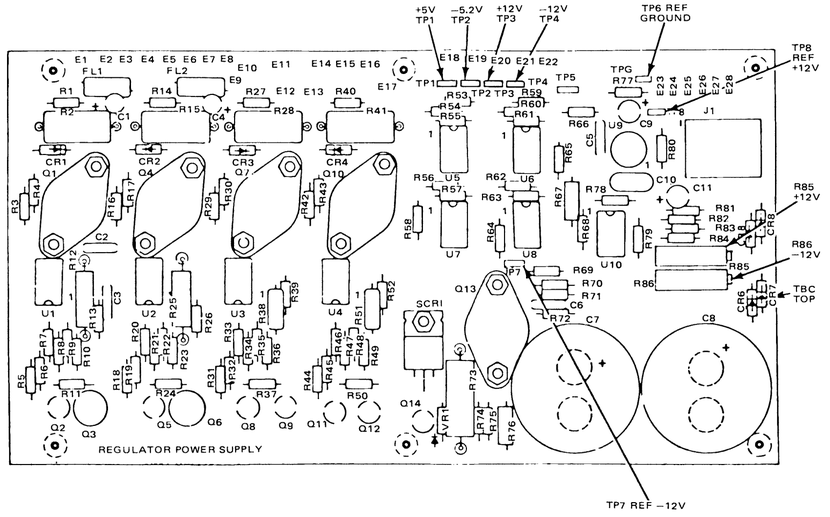
CIRCUIT	TYPE	AMPEX PART NO.	LOCATION
115V line	3A, Sb	070-002	Exposed rear of power supply (not functional in 625-line version)
230V line	1.5A, SB	070-993	Exposed rear of power supply
+5V supply	15A, FB	070-009	Heat sink inner wall

Power Supply Output Limits

SUPPLY	LIMIT	EXTENDER PWA TEST POINT
+12V	12.00 (± 0.01)V	Pin 1/2
-12V	12.00 (± 0.01)V	Pin 97/98
+5V	5.00 (± 0.05)V	Pin 9/10
-5.2V	5.2 (± 0.1)V	Pin 85

Power Jumper Positions

Line Voltage	POWER JUMPER POSITIONS	
	Line Selector Jumper	Range Jumper
95-110	115	Low
104-126	115	Medium
114-140	115	High
190-220	230	Low
208-252	230	Medium
229-279	230	High



Power Supply
Test and Maintenance Data
REFERENCE 2

SECTION 2
COLOR PROCESSOR
DESCRIPTION AND MAINTENANCE

2-1. INTRODUCTION

Refer to the following documents in the *Parts Lists and Schematics* manual:

ASSEMBLY No. 1405143

SCHEMATIC No. 1406117

Numbered data sheets (REFERENCE 1, 2, 3 . . . n) to which PWA descriptions and maintenance procedures refer are located at the end of this section as follows:

Overall Block Diagram – REFERENCE 1,2

Simplified Schematic – REFERENCE 3

Waveforms – REFERENCE 4

Maintenance Data – REFERENCE 5

COLOR PROCESSOR PWA 2 FUNCTION SUMMARY:

- The processed video output maintains a coherent relation between the subcarrier and the leading edge of the horizontal sync pulse (sync-coherent 3.58 MHz) for single-wire heterodyne EIAJ video and VPR slow-motion and still-frame modes of operation.
- For slow-motion and still-frame modes, the frame/2 signal from the VPR alternates the phase of the chroma signal to simulate a color frame.
- In the heterodyne mode the B–Y and R–Y components are decoded synchronously by locking a 3.58 MHz crystal VCO to the decoded R–Y component. The B–Y and R–Y components of the signal are then encoded using the sync-coherent 3.58-MHz clock from the Tape H Comparator PWA.

2-2. DESCRIPTION

The Color Processor PWA 2 performs a dual function. It permits the TBC to be used with a VPR in slow-motion and with a heterodyne VTR. The heterodyne VTR must be of the nonsegmented helical-scan type.

A heterodyne VTR produces a video output signal whose luminance component is sync-coherent but whose chrominance component is not sync-coherent. Before this signal can be time-base-corrected, the sync-coherence of the chrominance signal must be reestablished. The Color Processor PWA reestablishes a sync coherent chrominance signal by stripping chrominance from the video and demodulating chrominance with an off-tape-burst-derived 3.58-MHz subcarrier and then re-modulating the chrominance with a sync-coherent subcarrier. Chrominance is then added to luminance. This provides a video signal containing sync-coherent luminance and chrominance that will produce a standard NTSC signal after time-base correction.

During slow-motion and still-framing, the VPR plays back a single recorded field repeatedly. During slow-motion operation, a recorded field is played back many times before the next field is played back. As a result, the phase of the off-tape chroma may be identical field after field for long periods of time. This is inconsistent with NTSC requirements for a 180° phase reversal of the subcarrier between fields. When being supplied with still-frame or slow-motion video from a VPR the Color Processor PWA maintains correct chroma phasing necessary to simulate the four-field color frame of the NTSC signal. This is done by separating chrominance from luminance and then providing inverted and noninverted chrominance simultaneously at an electronic switch input.

This switch signal is provided by the Memory Control PWA 7 to either the inverted or non-inverted chroma.

2-3. Heterodyne Processing

When the NORMAL-HET switch on the TBC's front panel is set to HET, the Color Processor PWA processes off-tape video from a heterodyne-type VTR. The video signal from the VTR enters the color processor on PWA pin 21. The luminance low-pass filter and the chroma bandpass filter separate the video signal into its chrominance and luminance components. The off-tape luminance component from a heterodyne type VTR is not sync coherent. The luminance delay circuit delays the luminance by the same amount of time that the chroma processing circuits delay the chrominance. This ensures that the phasing of the two components is unchanged when they are added at the video amplifier. The chroma output of the chroma bandpass filter is separated into its B–Y and R–Y component in the B–Y and R–Y decoders, respectively. The decoders are synchronous detectors with the 3.58-MHz decoding signal developed from the off-tape burst.

B–Y and R–Y video components are encoded in B–Y and R–Y encoders which are balanced modulators. The carrier used in the encoding process is a sync-coherent 3.58-MHz signal developed by the Tape H Comparator PWA 5. Sync-coherent B–Y and R–Y components are summed together and form the required sync coherent chrominance. The chrominance is applied through switch U12 to current source Q27. The chrominance is then added to the luminance in the video output amplifier. The resulting sync-coherent video is passed through a 4.5-MHz low-pass filter and then through emitter-follower Q31 to PWA pin 81. The dc level of the video signal provided at PWA pin 81 is clamped by a feedback loop comprising sample-and-hold amplifier U14, Q24, and current source Q27. The sample-and-hold amplifier samples the level of the back porch and compares it with a reference value developed by potentiometer R189. The difference in the compared voltages is amplified and operates through the current source to alter the bias of the video output amplifier to establish the dc level. The sampling circuit in the sample-and-hold amplifier is driven by the clamp pulse driver U13/Q23 which amplifies the video clamp pulses applied to the PWA at pin 47 by the Tape VCO PWA 6.

The 3.58-MHz signal used by B–Y and R–Y decoders is generated by the crystal VCO. The phase of the 3.58-MHz signal is determined by the off-tape burst. Under timing control of the sync logic circuits, the crystal-controlled circuit samples the output of the R–Y decoder during burst time. The crystal oscillator maintains the phase of burst on a line-by-line basis. The burst is not H-sync-coherent. If the decoder oscillator follows the cyclic variations of burst phase, the chroma will be decoded to a true dc equivalent of the chroma phase vector. Reencoding of the chroma signal with the sync-coherent subcarrier establishes a chroma signal that can be processed by the TBC to produce a standard NTSC signal.

The sync-coherent 3.58-MHz driver receives the sync-coherent 3.58-MHz signal from the Tape H Comparator PWA 5, reshapes it into a sinusoid, and produces the 3.58-MHz-drive current required by B–Y and R–Y encoders.

2-4. Slow-Motion and Still-Framing Processing

When the NORMAL-HET switch on the TBC-2's front panel is set to NORMAL, the Color Processor PWA processes video from the VTR operating in slow motion or still frame. At tape speeds other than normal, the Color Processor PWA inverts the chroma component of the video as required to simulate the NTSC four-field color frame. Luminance and chrominance are separated as described previously in the paragraph on heterodyne processing. The chroma signal from the chroma bandpass filter is applied to a chroma inverter circuit. The chroma inverter circuit either inverts or transmits the chroma signal directly. Direct or inverted transmission through this circuit is under control of the frame/2 signal produced by the Memory Control PWA 8. During still-frame playback this signal is a 15-Hz square wave but the frequency is varied in proportion to the speed of the tape during slow-motion operation. The chroma is added to the luminance in the video output amplifier in the same way as during heterodyne processing.

2-5. COLOR PROCESSOR MAINTENANCE

See REFERENCE 4 and REFERENCE 5 in this section for the component locator diagram, jumper/test-point/adjustable-component summaries, and the waveforms called out in these procedures.

Before undertaking any adjustments to the Color Processor PWA review the *System Alignment Guide* (Table 3-2) and the *Tape/Reference Test Loop* discussion (Paragraph 3-5) in the *System Maintenance* section (Part I) for a general understanding of the nature and scope of these field adjustments.

Consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the color processor and interactive functions between it and other PWA's before making any adjustments.

2-6. Heterodyne Section Alignment

1. Use basic tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN.
2. With power off put color processor on an extender.
3. Chroma and subcarrier oscillator alignment:
   a. Adjust R22 (chroma level) fully clockwise for maximum chroma. This may be monitored at TP9 with oscilloscope triggered on pin 47 (clamp pulse).
   b. Switch burst off at signal generation.
   c. Set jumper J1 to B–C position.
   d. Connect oscilloscope or DVM to TP4 for a dc voltage measurement.
   e. Adjust R7 (crystal control offset) for +3.5 (± 0.5) Vdc.
   f. Return burst to test signal.
   g. Connect oscilloscope to TP3; trigger on internal.
   h. Set jumper J1 to A–B position.
   i. Adjust L2 (VCO peaker) for maximum subcarrier.
   j. Connect oscilloscope to TP7, internal trigger.
   k. Set MODE switch to HET.
   l. Adjust R144 (sync coherent subcarrier symmetry) and L8 (sync coherent subcarrier peaker) for maximum subcarrier.
4. Decode and encode circuit alignment:
   a. Set MODE switch to HET.
   b. Switch off R–Y chroma at the signal generator.
   c. Connect oscilloscope to TP8 and trigger from pin 47 (video clamp pulse in).
   d. Adjust R7 (crystal control offset) so that transition spikes shown in the bottom trace of WF16(J) are set to zero level as indicated in the top trace.
   e. Return R–Y chroma to test signal.
   f. Switch off B–Y chroma at the signal generator.
   g. Connect oscilloscope to TP10, trigger on pin 47.
   h. Adjust L3 (decode quadrature) to reduce transition steps to zero level. Bottom trace of WF17(K) shows a misadjustment L3; top trace shows correct adjustment.
   i. Return B–Y chroma to test signal.
   j. Connect oscilloscope to TP19, trigger on pin 47.
   k. Set R47 (R–Y gain) to mid-position.
   l. Adjust R48 (R–Y balance) and R108 (B–Y balance) for minimum rf on horizontal sync.

m. Connect channel A of vectorscope to TP19 or VIDEO OUT 1.

n. Trigger vectorscope on external subcarrier.

o. Switch R–Y off at signal generator.

p. Set vectorscope phase so that vector is aligned vertically at 90° on graticule.

q. Switch R–Y on, B–Y off at signal generator.

r. Adjust L14 (encode quadrature) so that vector is aligned horizontally at 180° on the graticule. This vector should be 90° from vector in step p.

s. Switch vectorscope to internal BURST ϕ REF.

t. Set jumper J1 to B–C position.

u. Set vectorscope gain to maximum.

v. Misadjust L1 (VCO frequency) slightly for an approximately 30-Hz beat of vector dot at center.

w. Adjust R48 and R108 for minimum circle around dot at center of vectorscope.

x. Set vectorscope gain to 75%.

y. Adjust L19 (chroma peaker) for maximum chroma as seen on vectorscope (or on oscilloscope connected to TP15).

z. Adjust R47 (R–Y gain) and L3 (decode quadrature) for minimum dot size at ends of vectors. A gross misadjustment of R47 is shown in WF18 (L).

aa. Adjust L1 for 5.0 Vdc at TP4.

2-7. Heterodyne/VPR Slow-Motion Output

NOTE

Chroma and luminance level controls are optimized at the factory for common slow-motion and heterodyne circuit functions. This procedure is used only to adjust chroma and luminance levels to accommodate a particular heterodyne VTR and to readjust chroma gain of the slow motion chroma inverter circuit for unity gain chroma of both circuit functions.

1. Normal output level adjustment:

   a. Use tape/reference test loop with a terminated oscilloscope looped through vectorscope channel A connected to VIDEO OUT 1. Switch signal generator video off for a color black signal.

   b. With power off extend Color Processor PWA.

   c. Switch MODE to HET.

   d. Observe one video line. Adjust R189 (clamp dc level) for zero blanking level. Slight tilt of video line should be averaged across zero and be the same for normal and heterodyne modes.

   e. Return 75% color bar to the input.

   f. Alternately select HET and NORMAL positions of MODE switch and adjust R193 (luminance level) for luminance in heterodyne to be the same as in normal.

   g. Alternately select HET and NORMAL positions of MODE switch and adjust R22 (chroma level) for chroma amplitude in heterodyne to be the same as in normal.

2. Chroma inverter adjustment:

   a. Select still frame at the VPR.

   b. Adjust L18 (chroma peaker) for maximum chroma level.

   c. Adjust R178 (chroma invert gain balance) for minimum dot bounce on vector display.

   d. Alternately select HET and NORMAL positions of MODE switch and adjust R223

(chroma invert gain) for chroma amplitude in heterodyne to be the same as in still frame (NORMAL position).

e. With power off return PWA to cage.

2-8. Filter Alignment

CAUTION

THIS PROCEDURE IS PROVIDED AS A REFERENCE ONLY AND SHOULD NOT BE ATTEMPTED WITHOUT A SPECTRUM ANALYZER AND VIDEO SWEEP GENERATOR. THERE SHOULD NOT BE ANY REQUIREMENT FOR A COMPLETE ALIGNMENT OF THE CHROMINANCE AND LUMINANCE FILTERS. EVEN FOLLOWING AN ACTIVE COMPONENT FAILURE, ALIGNMENT SHOULD BE RESTRICTED TO THE AFFECTED CIRCUIT.

1. Luminance and chrominance filter alignment:

a. Remove test signal from TAPE VIDEO IN connector.

b. Connect sweep generator to TP1. Set sweep generator for 1.5 Vp-p.

c. Connect spectrum analyzer to TP19.

d. Set MODE switch to HET.

e. Set jumper J2 to B–C position.

f. Set jumper J6 to B–C position.

g. Adjust L9 (luminance low-pass filter) for minimum 3.671 MHz.

h. Adjust L10 (luminance low-pass filter) for minimum 3.438 MHz.

i. Set jumper J8 to B–C position.

j. Adjust L15 (luminance low-pass filter) for minimum 1.576 MHz.

k. Return jumper J8 to A–B position.

l. Set jumper J10 to B–C position.

m. Adjust T1 (luminance low-pass filter) for minimum 1.576 MHz.

n. Return jumper J10 to A–B position.

o. Set jumper J7 to A–C position.

p. Set jumper J9 to B–C position.

q. Adjust L16 (luminance low-pass filter) for minimum 4.301 MHz.

r. Return jumper J9 to A–B position.

s. Set jumper J11 to B–C position.

t. Adjust T2 (luminance low-pass filter) for minimum 4.301 MHz.

u. Return jumper J11 to A–B position.

v. Return jumper J7 to A–B position.

w. Set MODE switch to NORMAL.

x. Connect oscilloscope to TP14.

y. Adjust L18 (chroma peaker) for peak in response at 3.58 MHz.

z. Set jumper J15 to B–C position.

aa. Adjust L23 (chroma invert filter) for minimum 3.891 MHz.

ab. Return jumper J15 to A–B position.

ac. Set jumper J16 to B–C position.

ad. Adjust T4 (chroma invert filter) for minimum 3.891 MHz.

ae. Return jumpers J2, J6, and J16 to respective A–B position.

af. Connect spectrum analyzer to TP9.

ag. Set MODE switch to HET.

ah. Adjust L6 (chroma band-pass filter) for minimum 2.000 MHz.

ai. Adjust L7 (chroma band-pass filter) for minimum 7.16 MHz.

2. Decode filter alignment:

a. Connect 75% color-bar test signal at standard level to TAPE VIDEO IN connector.

b. Connect oscilloscope to TP10.

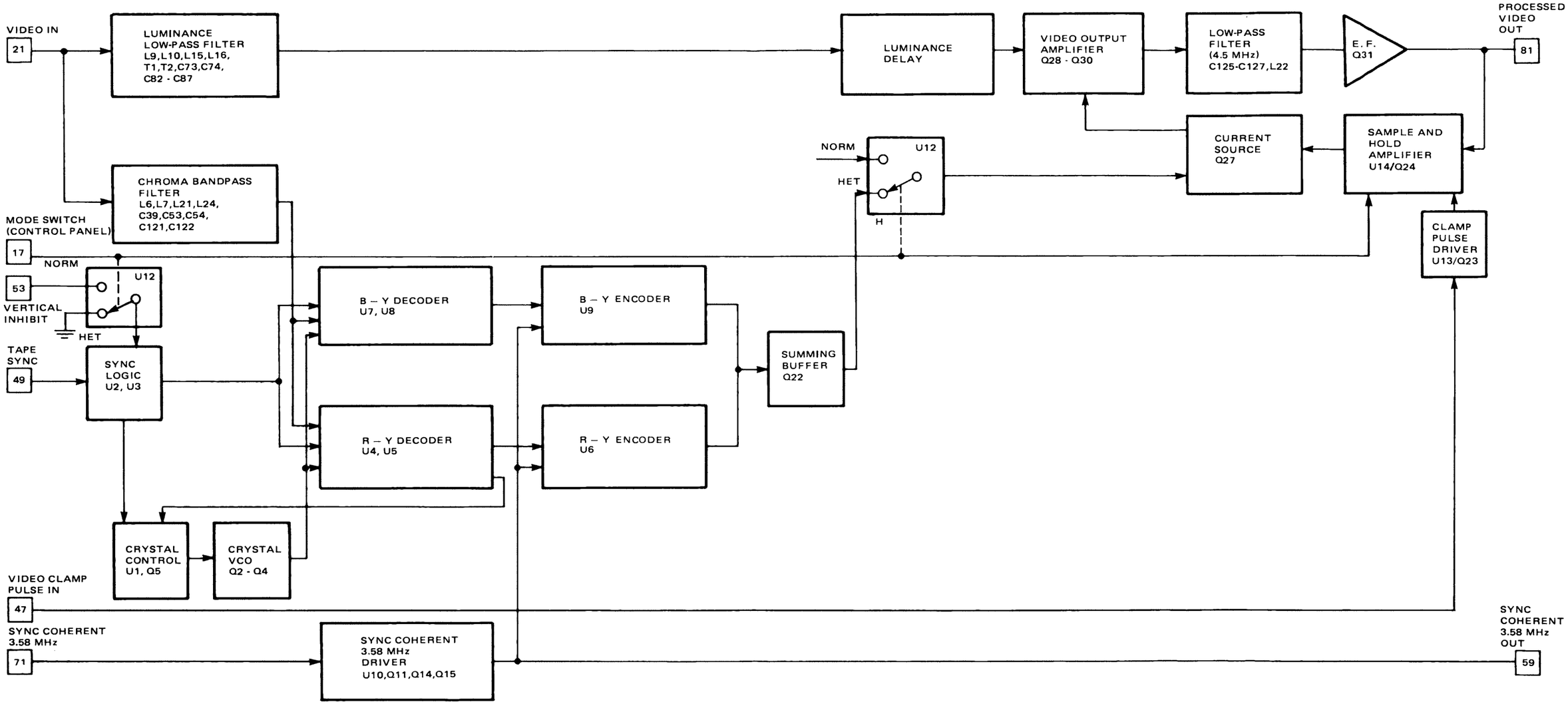
c. Trigger oscilloscope from pin 47 (video clamp pulse in).

d. Adjust L12 (B–Y decode filter) and L13 (B–Y decode filter) for squarest corner of greatest chroma transition (sharpest transition of chroma with no ringing or overshoots).

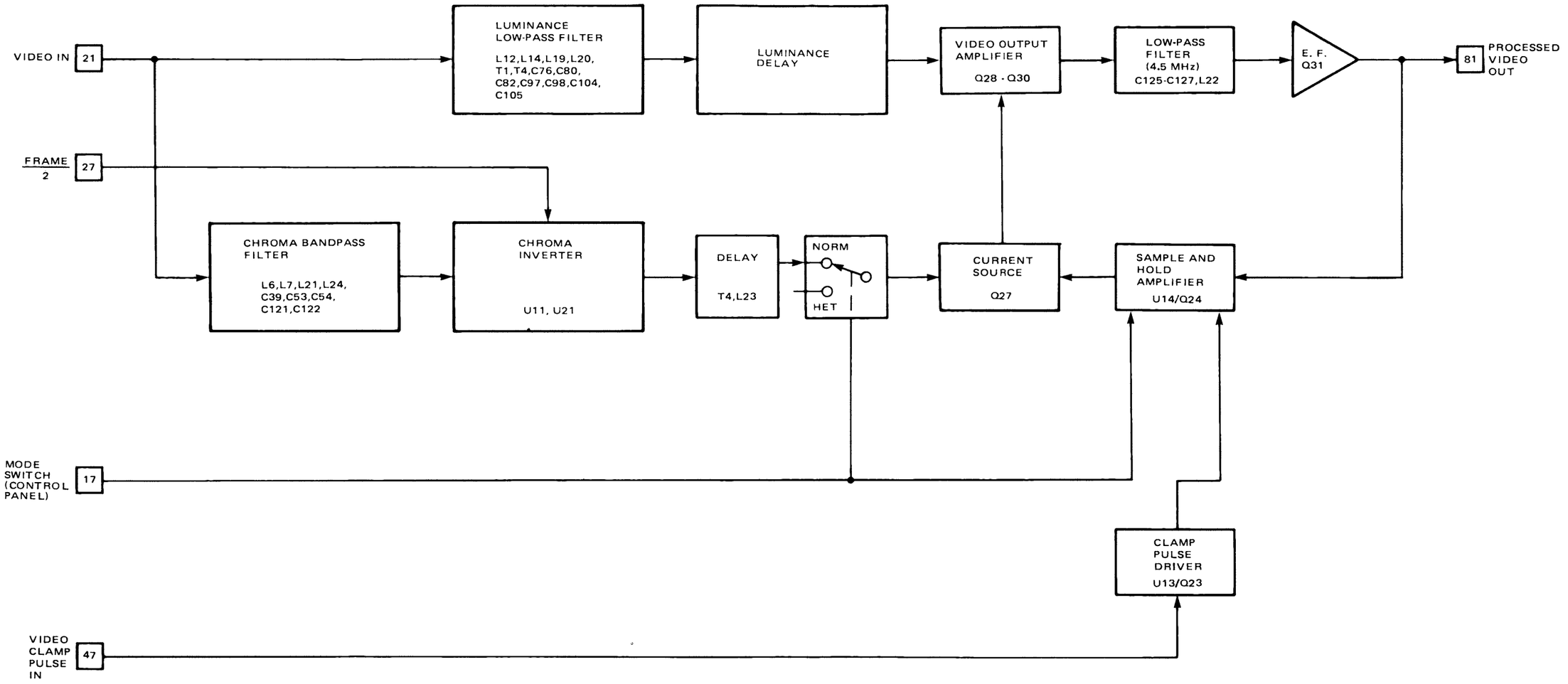
e. Connect oscilloscope to TP8.

f. Trigger oscilloscope from pin 47.

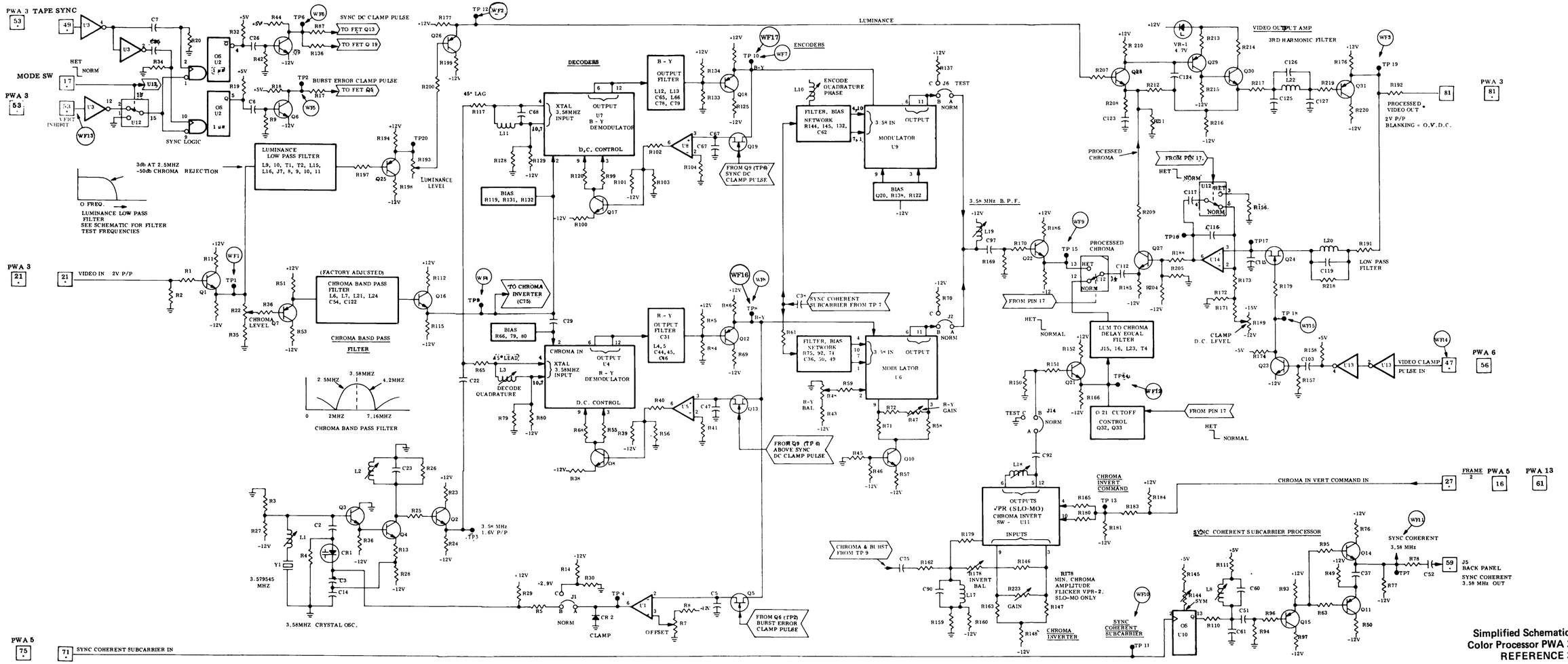
g. Adjust L4 (R–Y decode filter) and L5 (R–Y decode filter) for squarest corner of greatest chroma transition (sharpest transition of chroma with no ringing or overshoots).



Heterodyne Processing Mode Block Diagram,
Color Processor PWA 2
REFERENCE 1



Slow Motion Processing Mode Block Diagram,
Color Processor PWA 2
REFERENCE 2



Simplified Schematic, Color Processor PWA 2 REFERENCE 3

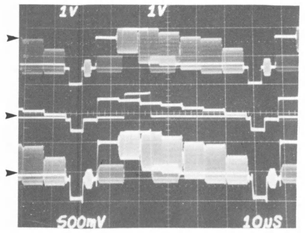
A

TP1
TAPE VIDEO IN
FROM PWA 3
WF1

TP12
LUMINANCE
WF2

TP19
COMPOSITE
VIDEO OUT
WF3

TRIG: TP2

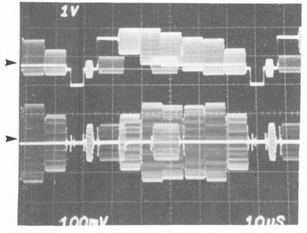


B

TP1
TAPE VIDEO
IN FROM PWA 3
WF1

TP9
CHROMA
WF4

TRIG: TP2



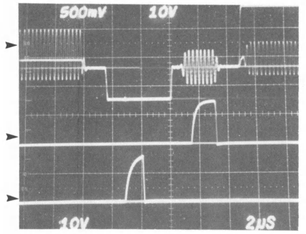
C

TP1
TAPE VIDEO
IN FROM PWA 3
WF1

TP2
BURST ERROR
CLAMP PULSE
WF5

TP6
SYNC DC
CLAMP
PULSE
WF6

TRIG: TP2



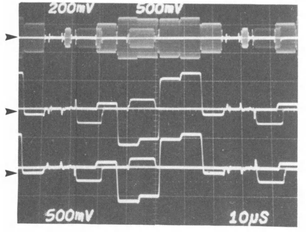
D

TP9
CHROMA
WF4

TP10
B-Y DECODED
WF7

TP8
R-Y DECODED
WF8

TRIG: TP2

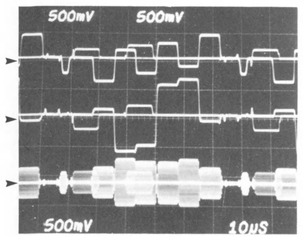


TP10
B-Y DECODED
WF7

TP8
R-Y DECODED
WF8

TP15
PROCESSED
(REMODULATED)
CHROMA
TRIG: TP2
MODE SWITCH: HET

E

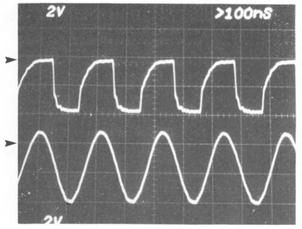


TP11
ENCODE Fsc
FROM PWA 6
WF10

TP7
SYNC COHERENT
3.58 MHz
WF11

TRIG: TP11

F

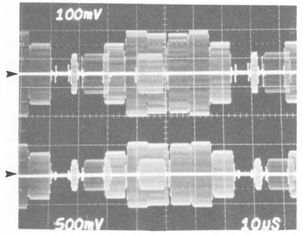


TP9
CHROMA
WF4

TP14
PHASE INVERTED
CHROMA
WF12

TRIG: TP3

G

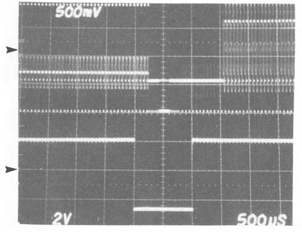


VIDEO IN
FROM PWA 3
WF1

PWA 7 PIN 53
VERTICAL INHIBIT
FROM PWA 7
WF13

TRIG: PIN 53

H



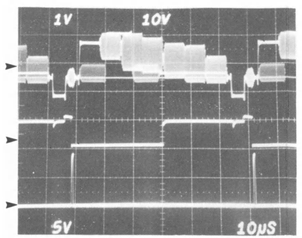
TP19
COMPOSITE
VIDEO OUT
WF3

PWA 2 PIN 47
VIDEO CLAMP
PULSE FROM PWA 7
WF14

TP18
CLAMP DRIVER
PULSE
WF15

TRIG: TP2

I

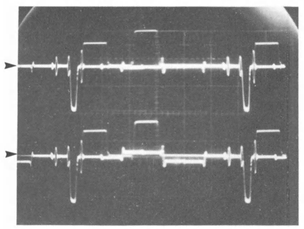


TP8
DECODED R-Y
NORMAL R7
ADJUSTMENT
WF16

R7 MISADJUSTED

TRIG: PIN 47

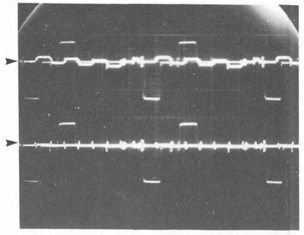
J



TP10
DECODED B-Y
NORMAL L3
ADJUSTMENT
WF17

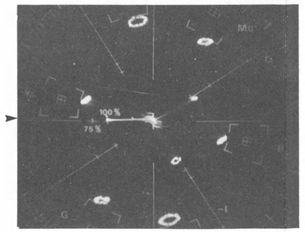
L3 MISADJUSTED

K



VECTORSCOPE
VIDEO OUT 1
R47 MISADJUSTED
WF18

L



Waveforms, Color Processor PWA 2
REFERENCE 4

AMPEX 1809474-01

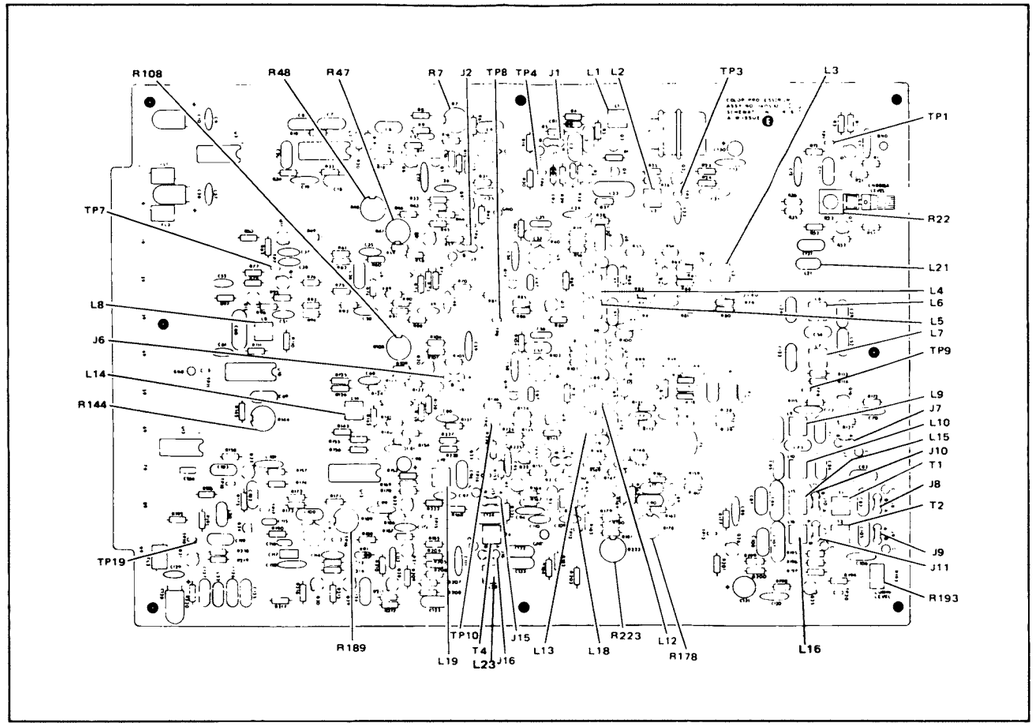
PWA 2 Jumpers

JUMPER	POSITION – FUNCTION	
J1	A–B	Normal
	B–C	Test–fixed error voltage to crystal oscillator
J2	A–B	Normal
	B–C	Test–removes R–Y encoder
J3		Not used
J6	A–B	Normal
	B–C	Test–removes B–Y encoder
J7	A–B	Normal
	A–C	Test–luminance low-pass filter alignment
J8	A–B	Normal
	B–C	Test–luminance low-pass filter alignment
J9	A–B	Normal
	B–C	Test–luminance low-pass filter alignment
J10	A–B	Normal
	B–C	Test–luminance low-pass filter alignment
J11	A–B	Normal
	B–C	Test–luminance low-pass filter alignment
J12		Not used
J13		Not used
J14	A–B	Normal
	B–C	Test–remove chroma inverter
J15	A–B	Normal
	B–C	Test–chroma invert delay filter alignment
J16	A–B	Normal
	B–C	Test–chroma invert delay filter adjustment

PWA 2 Adjustable Components

COMPONENT	FUNCTION
L1	VCO frequency
L2	VCO peaker
L3	Decode quadrature
L4(1)	R–Y decode filter
L5(1)	R–Y decode filter
L6(1)	Chroma band-pass filter
L7(1)	Chroma band-pass filter
L8	Sync coherent subcarrier peaker
L9(1)	Luminance low-pass filter
L10(1)	Luminance low-pass filter
L12(1)	B–Y decode filter
L13(1)	B–Y decode filter
L14	Encode quadrature
L15(1)	Luminance low-pass filter
L16(1)	Luminance low-pass filter
L18	Chroma peaker (Norm)
L19	Chroma peaker (Het)
L23(1)	Chroma invert filter
R7	Crystal control offset
R22	Adjusts chroma level
R47	R–Y gain
R48	R–Y balance
R108	B–Y balance
R144	Sync coherent subcarrier symmetry
R178	Chroma invert gain balance
R189	Clamp dc level
R193	Adjusts luminance level
R223	Chroma invert gain
T1(1)	Luminance low-pass filter
T2(1)	Luminance low-pass filter
T4(1)	Chroma invert filter

(1) Factory Adjustment Only – See reference procedure in Maintenance Section which uses a spectrum analyzer.



PWA 2 Component Locator

PWA 2 Test Points

TEST POINT	FUNCTION	TEST POINT	FUNCTION
TP1	Video input	TP12	Luminance
TP2	Burst error clamp pulse	TP13	Chroma invert frame/2
TP3	Decode subcarrier	TP14	Inverted chroma
TP4	Decode oscillator error	TP15	Processed chroma
TP6	Sync dc clamp pulse	TP16	Video clamp error
TP7	Sync coherent subcarrier output	TP17	Video clamp sample
TP8	R–Y chroma	TP18	Video clamp pulse
TP9	Chrominance	TP19	Processed video out
TP10	B–Y chroma	TP20	Luminance
TP11	Sync coherent subcarrier input		

Test Points, Jumpers, Adjustable Components, Component Locator, Color Processor PWA 2
REFERENCE 5

SECTION 3

VIDEO INPUT

DESCRIPTION AND MAINTENANCE

3-1. INTRODUCTION

Refer to the following documents in the *Parts Lists and Schematics* manual.

ASSEMBLY No. 1405134

SCHEMATIC No. 1405136

Numbered data sheets (REFERENCE 1, 2, 3 . . . *n*) to which PWA descriptions and maintenance procedures refer are located at the end of this section as follows:

Overall Block Diagram	– REFERENCE 1,2
Simplified Schematic	– REFERENCE 3,4,5
Waveforms	– REFERENCE 6,7
Maintenance Data	– REFERENCE 7

VIDEO INPUT PWA 3 FUNCTION SUMMARY:

- Provides black level clamping and amplification of off-tape video signal.
- Switches to enable direct video or processed EIAJ video from Color Processor PWA.
- Switches between input or TBC-processed video to the video monitor.
- Strips sync and burst from input video for processing in the Tape H Comparator PWA.
- Provides jumper-selectable test ramp signal.
- Contains video low, video overload, and color presence detectors.
- Detects search mode.

3-2. DESCRIPTION

The Video Input PWA accepts off-tape video from the associated VTR, amplifies the signal to a standard amplitude level, and clamps the back porch to a zero-volt reference level. When used with an Ampex VPR, the output video signal is routed to the Analog-to-Digital Converter PWA 4. In slow-motion or still mode, or when used with a heterodyne-process VTR, the signal is routed to the Color Processor PWA. After processing by PWA 2, the video signal is sent back to the Video Input PWA where black-level reference is inserted into the H-sync tip. The resultant video signal is then sent to the A/D Converter PWA.

The Video Input PWA also strips H-sync pulses from the video. These pulses are processed to produce various timing signals for use within the TBC system. Several antinoise features are provided to prevent incoming noise from introducing erroneous sync. Reference subcarrier (Fsc) burst is stripped from off-tape video and gated to the Tape H Comparator PWA 5. The presence or absence of burst is detected and converted to a TTL-level burst present signal.

The tape H-rate detector provides a TTL-level signal to indicate whether tape speed is less than or greater than ± 10% of normal. The two signals are AND'ed to produce a color present signal (color/mono) for use within the TBC and to kill the burst signal from the Video Output PWA 14 when burst is not present or when tape speed exceeds ± 10% of normal. Shuttle forward causes a net increase in tape H-rate; in shuttle reverse the result is a net decrease of tape H-rate. In slow motion or freeze the tape H-rate detector is not tripped because the net change of tape H-rate is only 1%.

If edit mute is operated or if no video is present the Video Input PWA provides a video mute signal to the Sync Generator PWA 15 to lock the blanking signal supplied to the Video Output PWA to the "on" condition, thereby blanking out the video display. Composite video from the Video Output PWA or off-tape video may be selected by the MONITOR/VIDEO switch for routing from the Video Input PWA to the MONITOR VIDEO OUT connector. Video overload and video low detectors provide signals to lamps on the control panel for indication of abnormal amplitude conditions in the Video Input PWA.

3-3. Tape H Control Signal Generator

See REFERENCE 1 and the timing waveforms. Off-tape video is amplified by X 5 amplifier U3 and stripped of chroma by the 3.58-MHz trap. The stripped video is inverted by buffer U12 and clamped to slice the tip of H-sync. Leading and trailing edges of H-sync are defined by one-shots which operate sample-and-hold circuits. The leading edge pulse samples the value of sync tip, the trailing edge pulse samples the value of back porch. Stored values are summed and used as a reference for the second sync slicer comparator. H-sync from amplifier U3 is compared with the summed reference in U36 to establish the 50% amplitude of sync.

Sample-and-hold circuits have a relatively long time constant. During the vertical inhibit signal from the Tape VCO PWA, sampling is inhibited, therefore the 50% slice level will not be disturbed by 2H pulses. If a dropout present signal is received from the serial-to-parallel converter, sampling will also be inhibited. Noise detector circuit U13, U14 is enabled by VCO lock from the Tape VCO PWA (search or not-qualified H). Comparator U13 references noise spikes generated by the VTR during high-speed operation against the stored sample of sync tip level and generates an inhibit signal which disables the second sync slicer and sample pulse generators.

Output of the second sync slicer is applied to the vertical broad pulse detector. The time constant of the circuit is such that narrow H and 2H pulses are suppressed and wide pulses of the vertical sync signal are detected. Output of the second sync slicer is also used to trigger the servoed pulse generator and sync rate detector circuits.

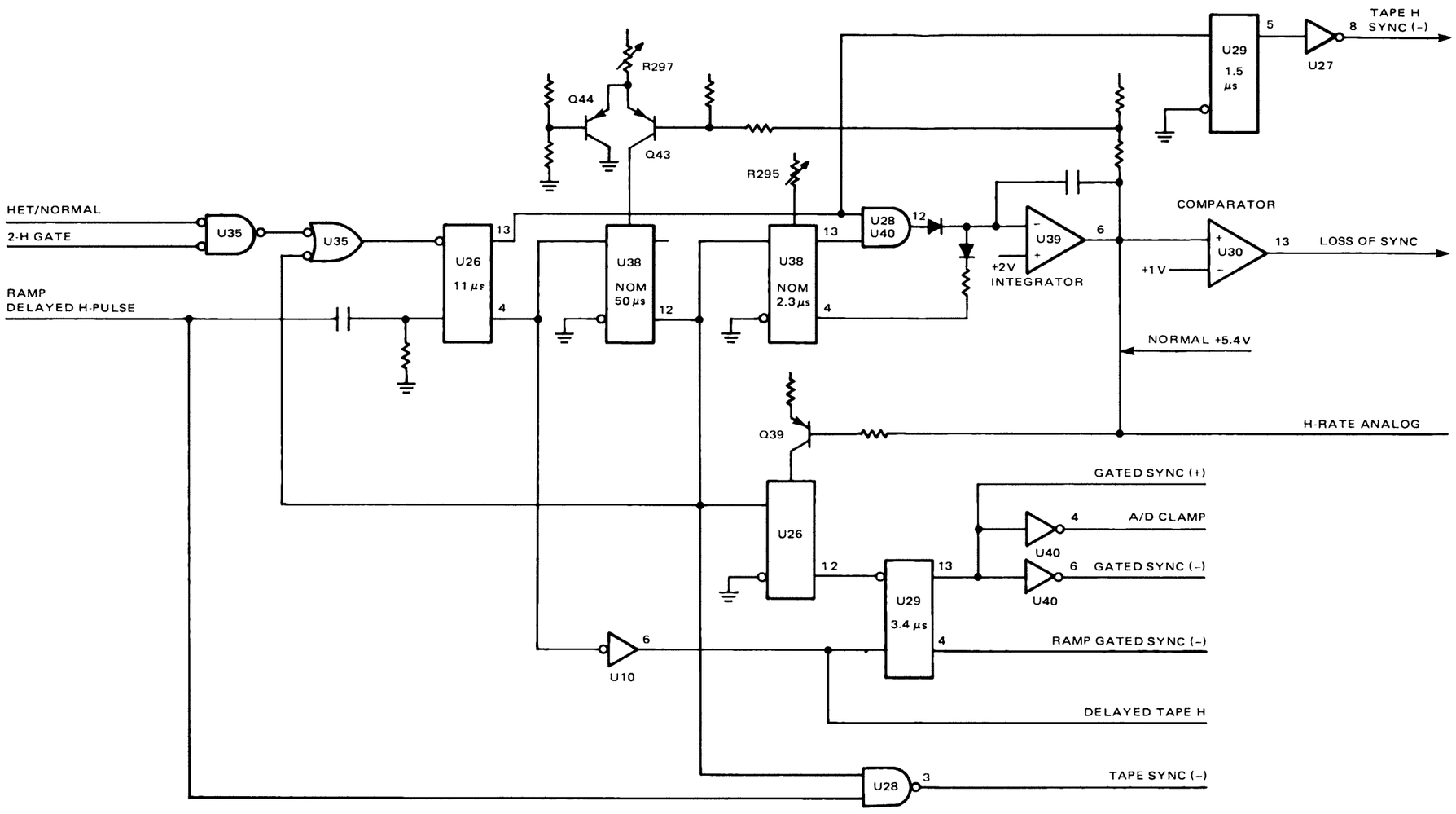
The ramp delay generator provides maximum delay of the sliced H-sync pulse when the color processor is in use (color-under VTR or slow-motion mode with the Ampex VPR) and minimum delay for normal color operation. This compensates for the additional delay of the video signal introduced by the color processor.

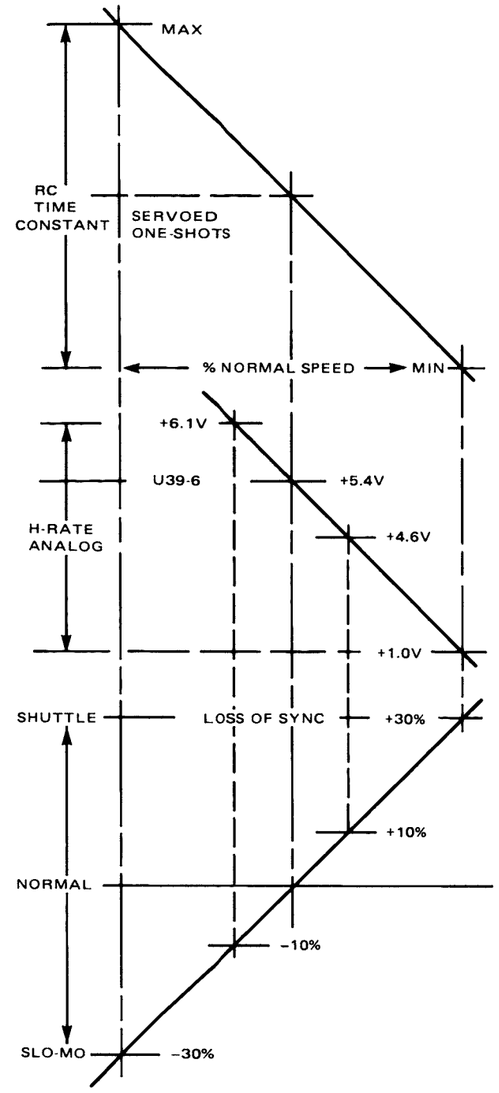
3-4. Servoed Pulse Generator and Sync Rate Detector

(See Figure 3-1, Servoed Pulse Generator and Sync Rate Detector, Simplified Schematic Diagram.) The function of the sync rate generator is (1) to provide system timing pulses derived from tape H-sync, (2) to provide an H-rate analog voltage proportionate to plus and minus 30% of normal tape speed, (3) to provide a less than or greater than ± 10% of normal H-rate TTL signal to kill the burst signal from the Video Output PWA if tape speed is greater than ± 10% of normal, and (4) to provide a loss of input signal if tape speed produces an H-rate in excess of plus 30% normal.

The sync rate generator is preceded by a servoed pulse generator circuit which prevents noise from entering the sync rate generator and being read as ramp-delayed H-pulses. The servoed pulse generator creates a window or period of time when a pulse can be gated through to the sync generator. The window enables the gating circuitry (window is open) only when a ramp-delayed H-pulse is expected to arrive. Gating circuits are disabled at all other times in the guarded interval between windows. This eliminates all noise pulses that may be present outside the window.

To provide a window for ramp-delayed H-pulses occurring at a constant rate, the most elementary circuit would be one which would inhibit the input for the time period between pulses. This could be done with a one-shot having a fixed time constant. Since the VPR can be operated in shuttle, slow-motion, and still modes, and because of time-base errors introduced in the recording/reproduction process, the guarded interval between ramp-delayed H-pulses must be servoed to track the





3356

Figure 3-1. Video Input PWA 3, Servoed Pulse Generator and Sync Rate Detector, Simplified Schematic Diagram

stretching and shrinking of the horizontal line period as tape speed varies. This is done by servoing the timing circuit of the guard interval producing one-shot to the repetition rate of the received ramp-delayed H-pulse. In this way, the period of the one-shot tracks changes in the repetition rate of the ramp-delayed H-pulses. The sync rate generator produces a voltage proportional to H-rate. This voltage is fed back to the timing circuit of one-shot U38 to produce the required servo or tracking action. Operation of the circuit is as described in the following paragraphs. (See Figure 3-1, Servoed Pulse Generator and Sync Rate Detector, Simplified Schematic Diagram.)

The 2H gate from the VPR-2 via U35 inhibits incoming half-line 2H pulses during the vertical blanking interval and permits pulses that define the H-period to be passed. In heterodyne mode the 2H input is blocked.

The ramp-delayed H-pulse triggers an 11-microsecond one-shot, U26, and the trailing edge of the pulse at U26-4 triggers a servoed one-shot, U38, which has a nominal time-constant of 50 microseconds. The input one-shot, U26-4, is inhibited during this period. The trailing edge of the pulse at U38-12 triggers a nominal 2.3-microsecond one-shot U38-4. The positive pulse from U26-13 overlaps the positive pulse from U38-13 throughout the operating range of the shuttle mode of operation, with minimum overlap at –30% H-rate and maximum overlap at +30% H-rate. The integrating capacitor across U36 receives maximum positive charge at –30% H-rate and minimum positive charge at +30% H-rate. Voltage developed at U39-6 determines the charge rate of the RC circuit of U38 controlled by Q43. Thus, a window of approximately 13 microseconds is provided for the incoming H-pulse to guard against noise. The same H-rate analog voltage is applied to Q39 to guard the input to U29-4. The H-rate analog voltage is also applied to a comparator, U30, which will trip if the analog voltage falls below +1 volt, indicating sync not present.

3-5. Video Switching and Processing

See REFERENCE 2. The function of the video switching and processing circuits is (1) to route tape video input either directly to the A/D Converter PWA (normal operation) or to the Color Processor PWA (slow-motion mode with the VPR, or color-under VTR), (2) to gate subcarrier burst out to the Tape-H Comparator PWA, (3) to provide a TTL color-present signal to designate tape H-rate less than ± 10% of normal AND burst present, or tape H-rate greater than ± 10% of normal OR burst not present, (4) to provide control panel indication of abnormal video amplitude conditions in the Video Input PWA (video overload, video low), (5) to provide selection of monitor video display of tape video input or TBC-2 composite video output, and (6) to provide an internally generated ramp for calibration of the system video processing circuits.

3-6. Input Video Amplifier

The tape video input amplifier, Q1 to Q7, is calibrated to provide a 2-volt peak-to-peak output (sync tip to white color-bar tip). The clamp pulse generator circuit, U14, U15, U16, will clamp the back porch to a reference 0 volts. The clamp circuit is inhibited by loss of sync signal from the H-rate analog circuits, and vertical (+) from the Tape VCO PWA. VPR's without the sync head option will have a vertical dropout during the vertical blanking interval and will not provide sync at that time. When the TBC is used with a color-under VTR, noise bursts at the beginning of the vertical blanking interval are encountered which can upset the TBC circuits.

3-7. Video Input Switch

In the Tape VCO PWA, the color present signal is gated with het/normal, search (–), and slow motion to produce the video input switch signal. If the conditions are in color and heterodyne mode, or color and slow motion, then switches U6 and U1 will select the 2-volt peak-to-peak video from the Color Processor PWA. (See REFERENCE 2, *Video Switching and Processing,* Simplified Block Diagram.) In normal mode, as selected by the mode switch on the control panel, or in monochrome condition (burst not present or tape H-rate greater than ± 10%) or in search condition (tape H-rate higher than the operating range of the 6-Fsc oscillator on the Tape VCO PWA), the output of the video input amplifier, Q1 to Q7, will be selected. Selected video will be routed to the remaining circuits of the Video Input PWA.

3-8. Video Output to the A/D Converter A PWA 4

Selected video is routed through a low-pass filter (0 to 6 MHz) to the output buffer amplifier, Q11 to Q13, which drives the A/D reference insert amplifier switch. The A/D reference is inserted into the horizontal sync to establish an arbitrary –30 IRE-unit reference level within the TBC. In the editing process, not all program material will necessarily have the same standard of sync tip level, therefore an internal standard is imposed to provide a reference level for the video signal. See REFERENCE 6, WF4(B) which shows the insert level on the sync tip at PWA pin 78 (for 75% color-bar input). Nominal level at pin 78 is 1980 mVp-p from sync tip insert to 100% saturated color (equivalent to –30 to +139 IRE units) to match the 2-volt A/D conversion range with sufficient headroom for best S/N. The A/D reference insert switch is operated by the gated sync (+) from the servoed pulse generator. Black level control from the control panel permits adjustment of the black level value to suit studio conditions.

3-9. Burst and Color Present Circuits

Tape video input, whether directly from the input video amplifier or via the color processor, is amplified by the chroma amplifier and gated by U17 switch. Tape sync (–) from the servoed pulse generator circuits triggers a 3.3-microsecond one-shot. During the 3.3-microsecond period (when the burst is gated through) the burst passes through the burst filter out to the Tape H Comparator PWA.

Burst is also applied to the burst threshold detector and is gated through to the integrator comparator, U21, by gated sync (–) from the servoed pulse generator circuits. The resultant burst present/not present signal is AND'ed with the greater than/less than ± 10% tape H-rate signal to produce the color present signal. Color present is used in the Sync Generator PWA to kill the burst signal output of the Video Output PWA. It is also used for other functions related to tape H-rate in the Tape H Comparator PWA and the Tape VCO PWA. Within the Video Input PWA the video input switch signal from the Tape VCO PWA (which is derived in part from the color present signal) determines whether the Color Processor PWA is used or not.

3-10. Test Ramp Generator

An internally generated test ramp is provided for maintenance and calibration of the TBC system video processing circuits. The test ramp can be substituted for the tape video input by reconnecting jumper J4. The test ramp is triggered by ramp-delayed H-pulse from the servoed pulse generator.

3-11. Video Low Detector and Video Overload Detector

The video low detector U9-13 is held high by continuous retriggering of the one-shot by ramp-delayed tape H from the servoed pulse generator. If the video signal amplitude falls too low, comparator U8 will inhibit U9, causing the video low lamp on the control panel to light. If the video amplitude becomes too high, comparator U7 will trigger U9-12, causing the video overload light on the control panel to light.

3-12. Monitor Video Circuit

The monitor driver, Q23 through Q26, delivers tape video input (2 volts peak-to-peak) or TBC video from the Video Output PWA to the back panel for use by the monitor as selected by the monitor switch on the control panel.

3-13. VIDEO INPUT MAINTENANCE

See REFERENCE 6 and REFERENCE 7 in this section for the component locator diagram, jumper/test-point/adjustable-component summaries, and waveforms called out in these procedures.

Before undertaking any adjustments to the Video Input PWA review the *System Alignment Guide* (Table 3-2) and the *Tape/Reference Test Loop* discussion (Paragraph 3-5) in the *System Maintenance* section (Part I) for a general understanding of the nature and scope of these field adjustments.

Consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the Video Input PWA and interactive functions between it and other PWA's before making any adjustments.

3-14. Video Input Adjustment

1. Use basic tape/reference test loop setup with a 75% color-bar test signal at standard level to TAPE VIDEO IN.

2. With power off put the Video Input PWA on an extender.

3. Video level adjustment:

   a. Connect oscilloscope to TP2; trigger on TP8.

   b. Adjust R6 (video in gain) for 2.0 Vp-p video.

4. Sync delay adjustment:

   a. Connect oscilloscope –

      Channel 1: TP9

      Channel 2: TP15

      Trigger: TP15

   b. Adjust R239 (sync delay) so that the positive edge of the pulse at TP9 lags the negative edge of the pulse at TP15 by 0.96 microseconds. See WF24/25(M).

   c. Set Mode switch to HETERODYNE.

   d. Verify that the interval in step b shifts to 1.8 (± 1.0) microseconds.

   e. Return MODE switch to NORMAL.

5. Sync gate servo adjustment:

   a. Connect channel 1 of oscilloscope to TP16; trigger on internal.

   b. Adjust R295 (search servo recovery) for a positive pulse width of 2.3 microseconds.

   c. Connect channel 1 of oscilloscope to U39 pin 6; trigger from line.

   d. Adjust R297 (search color detector) for +5.5 Vdc.

   e. Connect oscilloscope –

      Channel 1: TP14

      Channel 2: TP9

      Trigger: TP14

   f. Connect VPR output to TAPE VIDEO IN.

   g. Verify that positive pulses on channel 2 occur during negative pulses of channel 1. Vary VPR shuttle speed and verify that pulses on channels 1 and 2 stay locked to each other, for a period on channel 1 from 40 microseconds to 150 microseconds.

   h. Set shuttle speed full counterclockwise. Verify that video mute (PWA pin 31) is low.

   i. Reconnect signal generator to TAPE VIDEO IN.

6. Burst gate and burst phase adjustment:

   a. Connect oscilloscope –

      Channel 1: TP1

      Channel 2: TP 4

      Trigger: TP8

   b. Adjust R244 (burst gate) so that the positive edge of the pulse at TP4 lags the negative edge of sync at TP1 by 5.0 microseconds.

   c. Connect oscilloscope –

      Channel 1: TP5

      Trigger: TP8

   d. Switch burst off at signal generator.

   e. Adjust R186 (burst amplifier balance) for minimum error (best straight line).

f. Return burst to input video.

g. Connect vectorscope channel A to PWA pin 67/68. Trigger internally.

h. Adjust inductors L8 and L9 (burst filter) for maximum burst amplitude.

i. Retune L8 and L9 for best burst phase.

NOTE

Optimum phasing is indicated by a solid line burst vector where out-of-phase loop shown in WF26(N) is closed to a solid line as shown in WF27(N). The slight loop shown in WF27(N) is the normal condition and is a compromise between heterodyne and normal mode burst vectors. If the TBC is to be used only in normal or only in heterodyne mode, the burst vector may be adjusted for a solid line to optimize phasing range in that mode.

j. With power off return PWA to its slot.

3-15. Video Filter Response

NOTE

The following procedure is for reference only and should not be attempted without proper test equipment.

1. Remove shielded cable at E1/E2.
2. Connect sweep generator to E1/E2.
3. Connect spectrum analyzer to TP3.
4. Ground TP10.
5. Install J1 to A–B and remove J2.
6. Adjust inductor L1 for a minimum response at 7.159 MHz.
7. Adjust L2 for a minimum response at 9.852 MHz. There is interaction between L1 and L2. Perform steps 6 and 7 several times to obtain minimum 7.159 MHz and 9.852 MHz.
8. Install J2 to A–B.
9. Adjust L3 for minimum response at 4.803 MHz.
10. Remove jumper J1 and jumper J2.
11. Adjust T1 for minimum response at 4.803 MHz.
12. Install J2 to A–B.
13. Verify that response from 0 MHz to 4.0 MHz is +0.1 dB (referenced to response at 1.0 MHz).
14. Adjust L1 slightly for response at 7.159 MHz to be –45 dB from response at the 1.0 MHz reference.
15. Verify that response from 7.2 MHz to 11 MHz is –25 dB from response at 1.0 MHz reference.
16. Remove ground from TP10.
17. Reconnect shielded cable to E1/E2.
18. Connect shield to E2.

3-16. VPR-20 Interface

Some later TBC-2B's may have the VPR-20 interface circuit kit which detects the first two equalizing pulses to provide vertical timing consistent with normal internal TBC vertical timing. Adjust timing as follows:

1. Setup normal VPR-20 configuration to play back standard 75% color bars.

2. With power off extend Video Input PWA.

3. Switch VPR-20 vertical switch on PWA edge on (up).

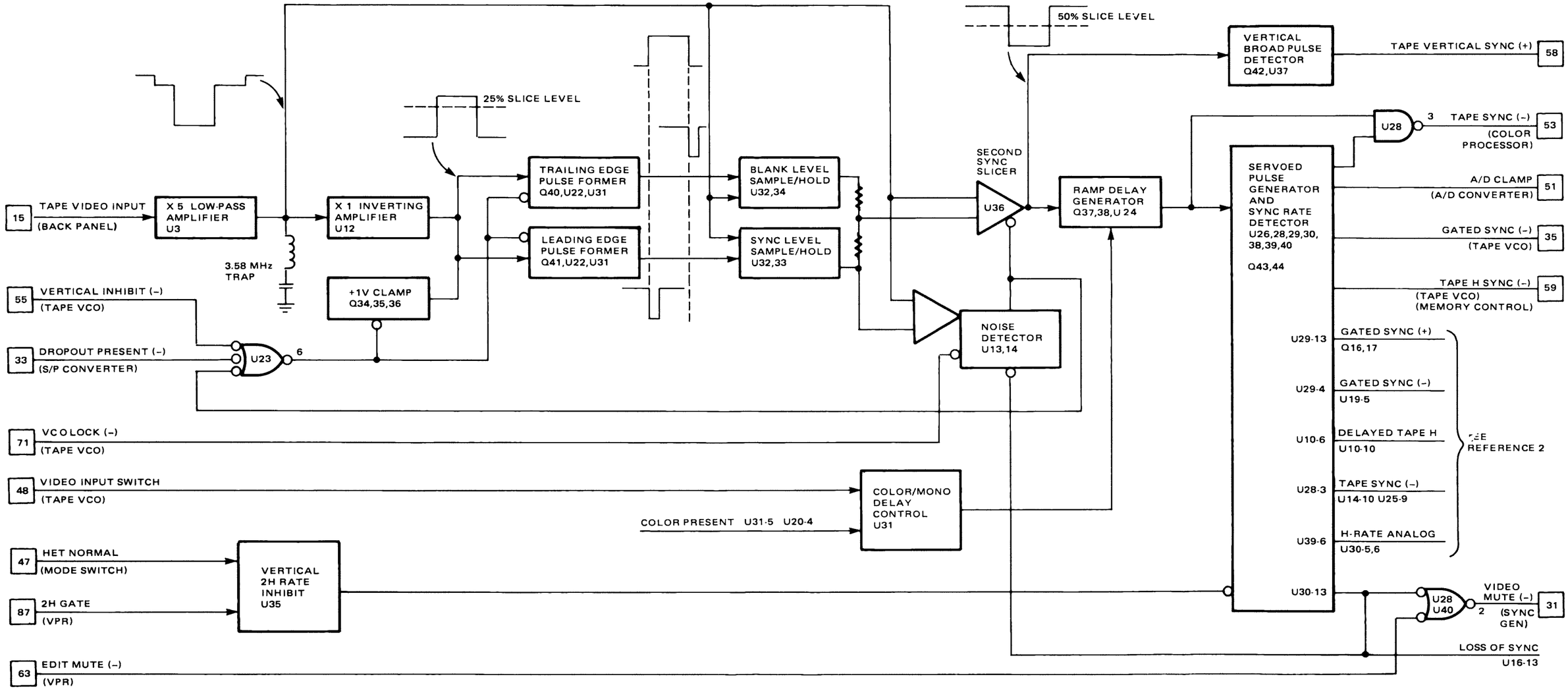
4. Connect oscilloscope –

   Channel 1: TP9 (Delayed stripped sync)

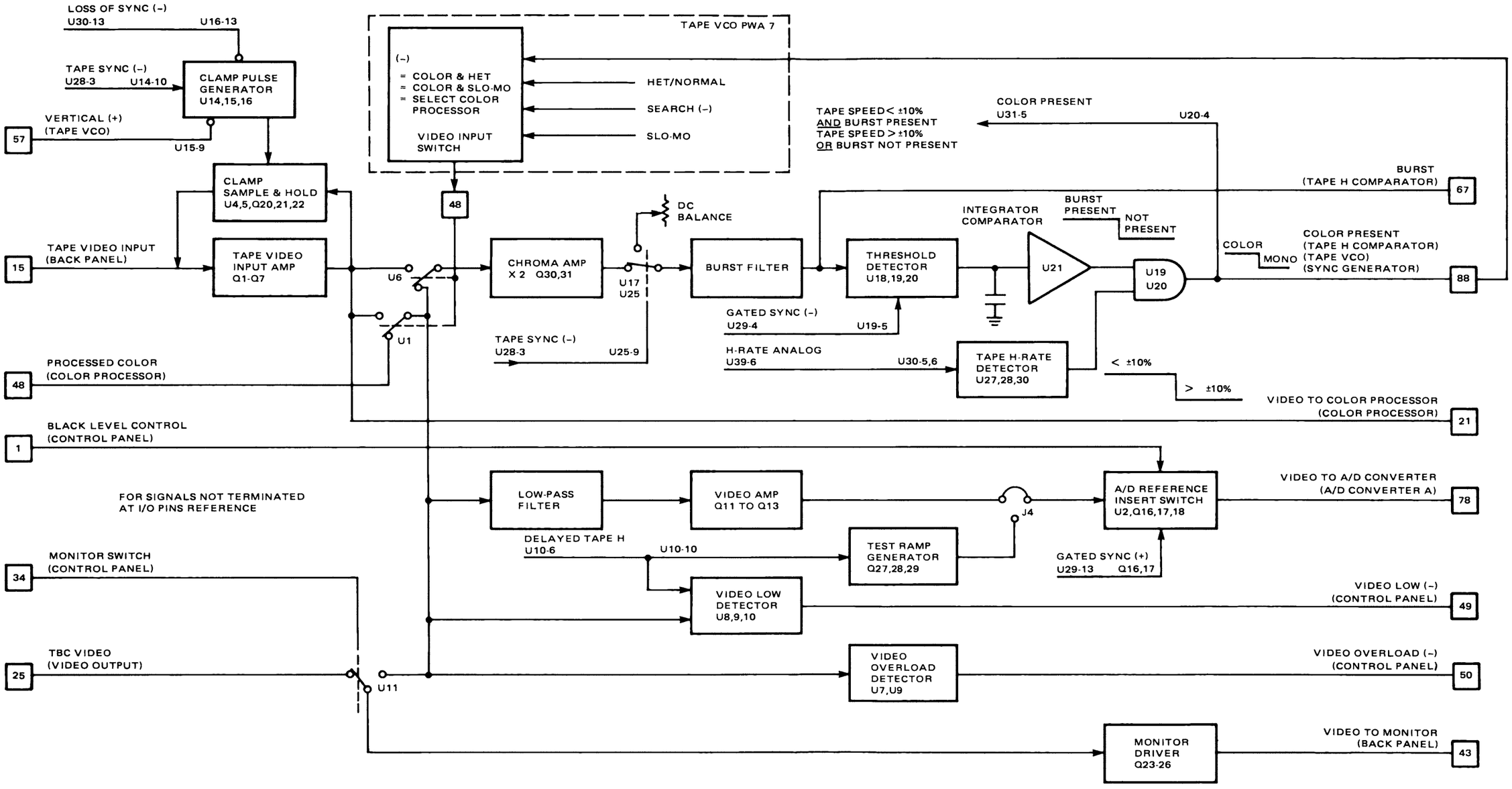
   Channel 2: PWA Pin 58 (Tape vertical)

   Trigger: TP9

5. Play tape and adjust R6 on the interface board so that leading edge of positive pulse at pin 58 is delayed 5 microseconds from start (negative edge) of the off-tape first vertical broad pulse at TP9.

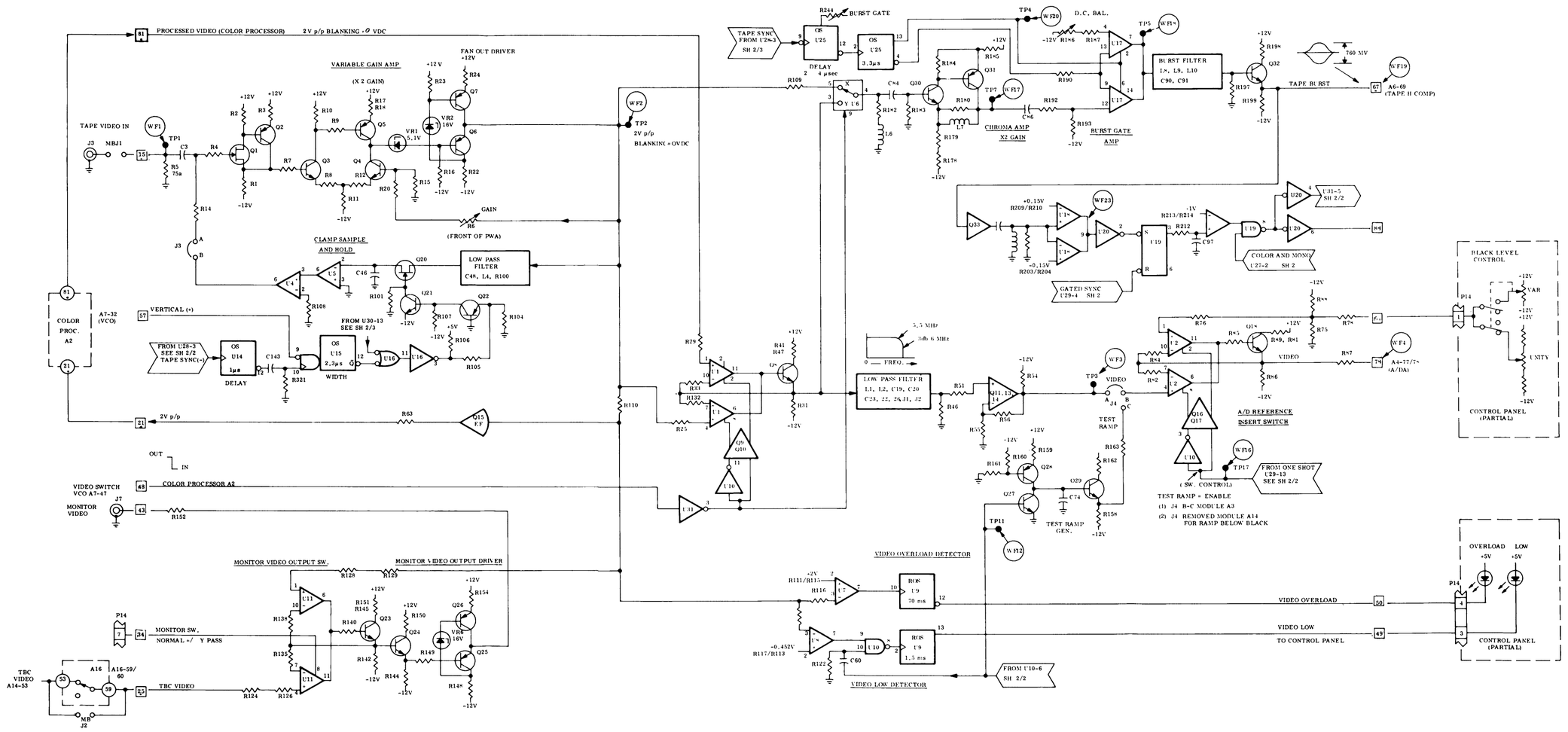


Tape H Signal Generator Circuits
Video Input PWA 3 Block Diagram
REFERENCE 1

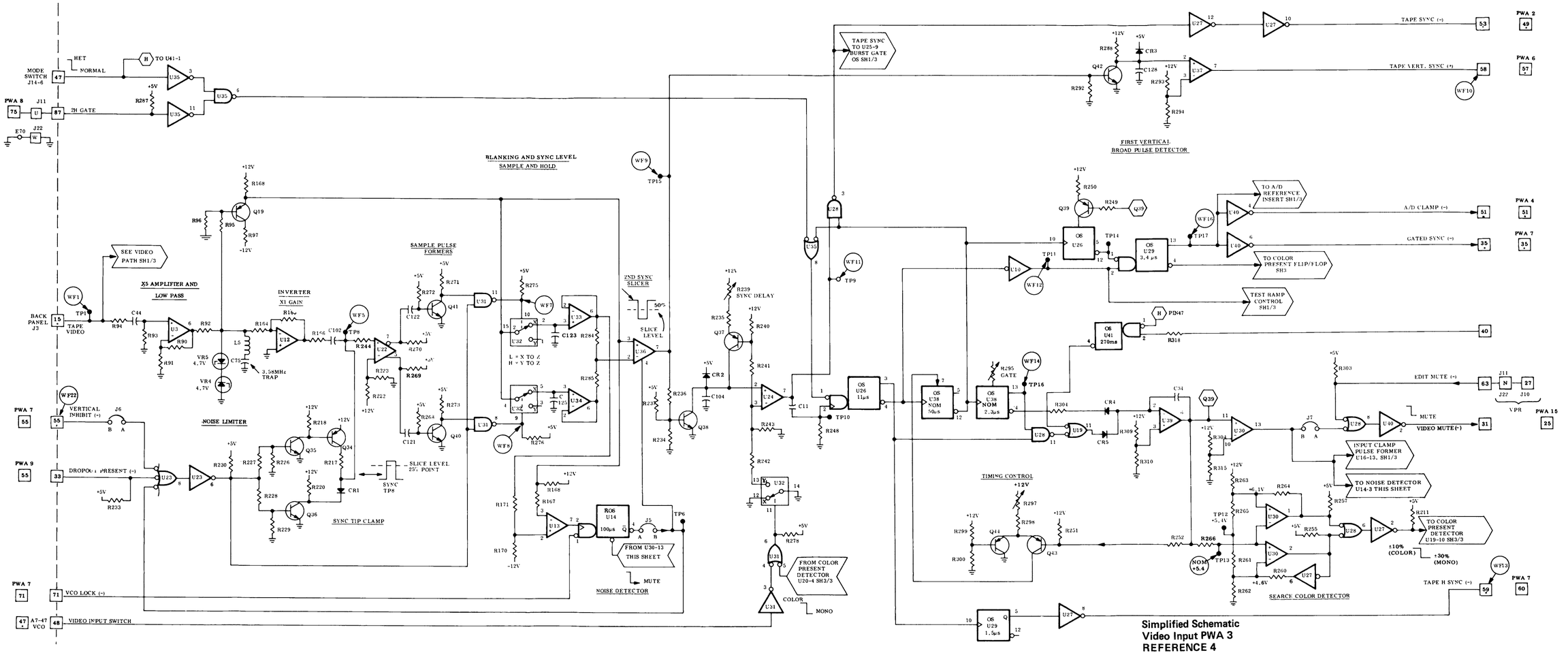


Video Input PWA 3,
Video Switching and Processing
Block Diagram
REFERENCE 2

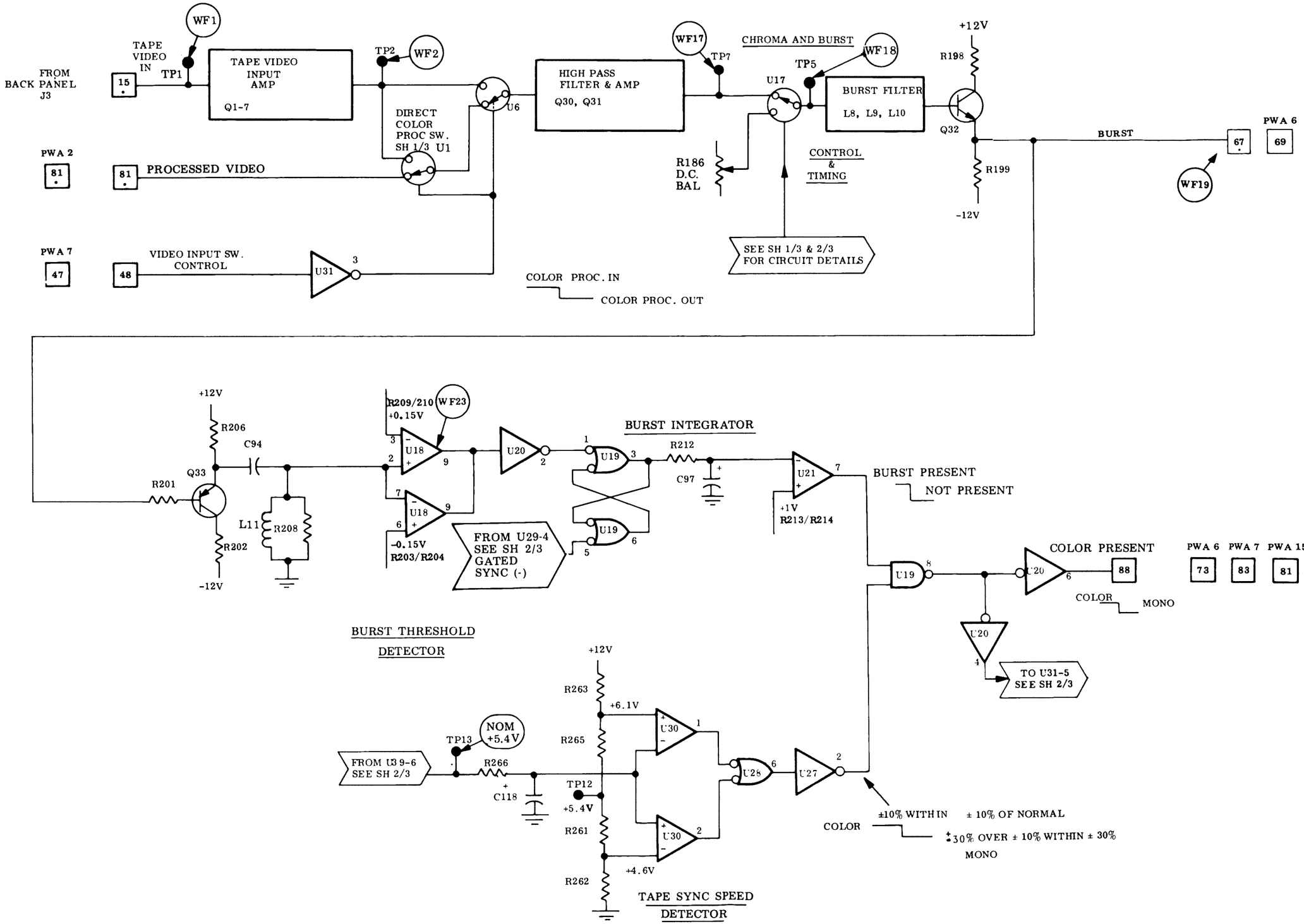
AMPEX 1809474-01



Simplified Schematic
Video Input PWA 3
REFERENCE 3
(1 of 3)



Simplified Schematic
Video Input PWA 3
REFERENCE 4
(2 of 3)



Simplified Schematic
Video Input PWA 3
REFERENCE 5
(3 of 3)

A

TP1
TAPE VIDEO
INPUT PWA 3

WF1

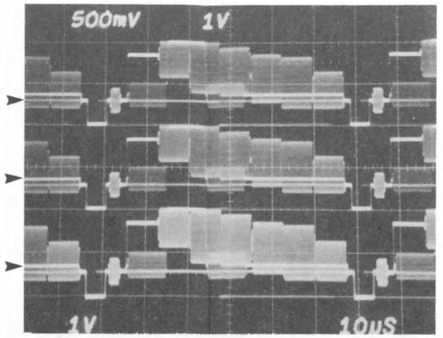
TP2
VIDEO AMPLIFIER
OUTPUT (Q7)

WF2

TP3
LOW-PASS FILTER
AMPLIFIER OUT-
PUT (Q13)

WF3

TRIG: PIN 51



B

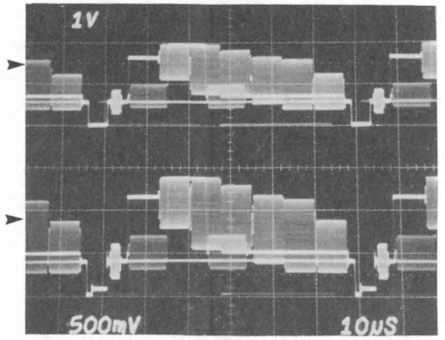
TP3
LOW-PASS FILTER
AMPLIFIER OUT-
PUT (Q13)

WF3

PWA 3 PIN 78
VIDEO OUTPUT
TO A/D

WF4

TRIG: PIN 51



C

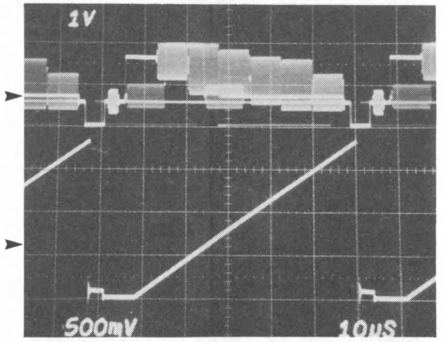
TP3
LOW-PASS FILTER
AMPLIFIER
OUTPUT (Q13)

WF3

PWA 3 PIN 78
TEST RAMP VIDEO
OUTPUT TO A/D

WF4

TRIG: PIN 51
TEST RAMP: J4 B–C



D

TP1
TAPE VIDEO
INPUT

WF1

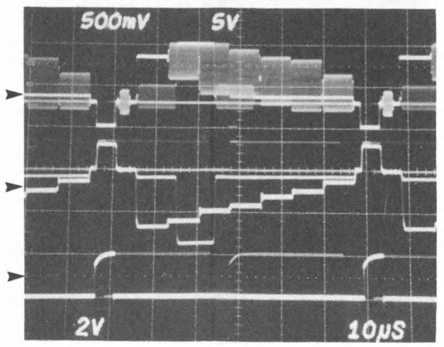
TP8
INVERTING
AMPLIFIER OUT-
PUT (CHROMA
STRIPPED)

WF5

U29-5
TAPE H SYNC (+)

WF6

TRIG: PIN 51



TP8
INVERTING
AMPLIFIER
OUTPUT

U31-11
LEADING EDGE
SAMPLE PULSE
FORMER

U31-8
TRAILING EDGE
SAMPLE PULSE
FORMER

TRIG: PIN 51

TP8
INVERTING
AMPLIFIER
OUTPUT

TP15
SECOND
SYNC SLICER

PWA 3 PIN 58
TAPE VERTICAL
SYNC (+)

TRIG: PIN 58

TP15
SECOND SYNC
SLICER

TP9
RAMP DELAYED
SYNC

TP11
RAMP DELAY
TAPE H TRIGGER

TRIG: PIN 51

TP9
RAMP DELAYED
SYNC

PWA 3 PIN 59
TAPE H SYNC
(–) OUTPUT

TP16
SERVO GATE

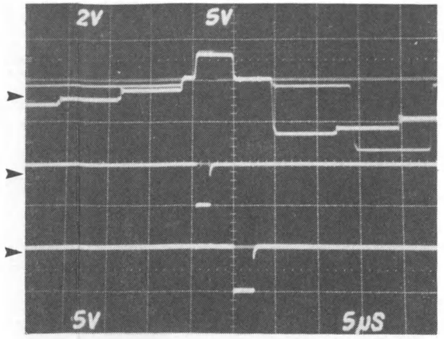
TRIG: PIN 51

E

WF5

WF7

WF8

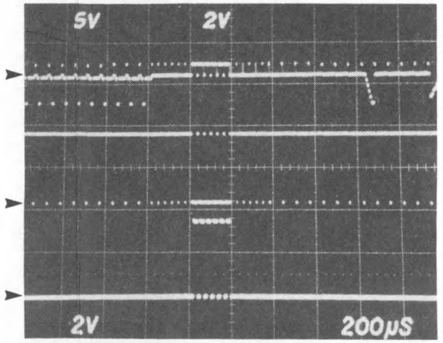


F

WF5

WF9

WF10

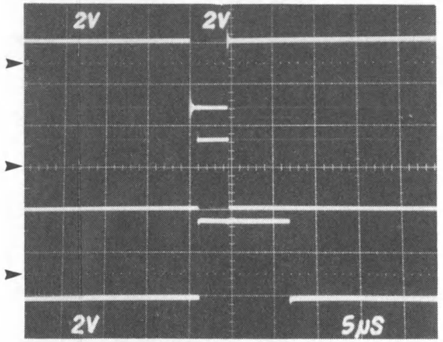


G

WF9

WF11

WF12

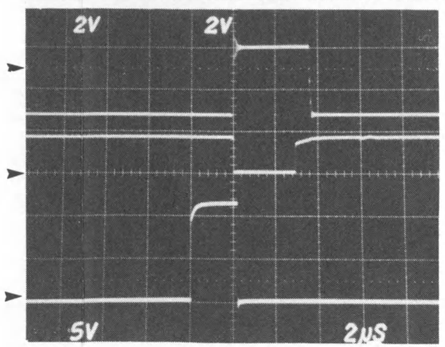


H

WF11

WF13

WF14



I

TP1
TAPE VIDEO INPUT

WF1

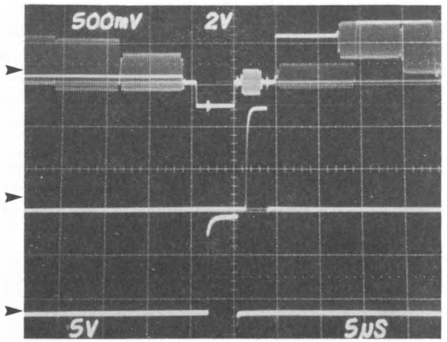
CLAMP SAMPLE
AND HOLD DRIVE
COLLECTOR Q21

WF15

TP17
A/D REFERENCE
INSERT SWITCH
DRIVE

WF16

TRIG: PIN 51



J

TP7
CHROMA AMPLIFIER
OUTPUT

WF17

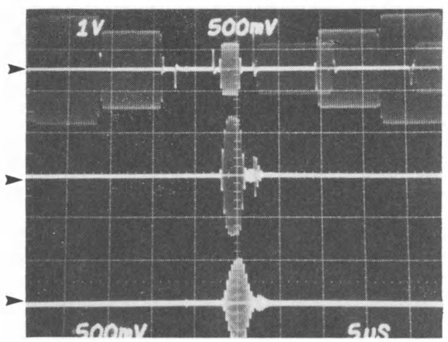
TP5
BURST GATE
OUTPUT

WF18

PWA3 PIN 67
BURST OUTPUT

WF19

TRIG: PIN 51



K

TP7
CHROMA
AMPLIFIER
OUTPUT

WF17

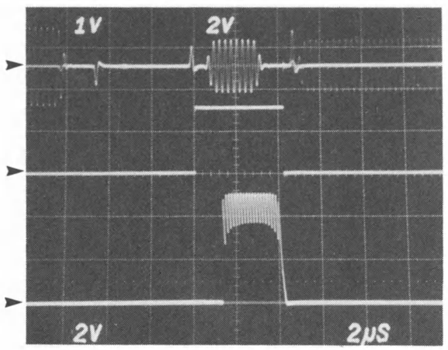
U25-13
BURST GATE
ONE-SHOT

WF20

U18-9
BURST THRES-
HOLD DETECTOR

WF23

TRIG: PIN 51



Waveforms, Video Input PWA 3
REFERENCE 6

L

TP1
TAPE VIDEO
INPUT

WF1

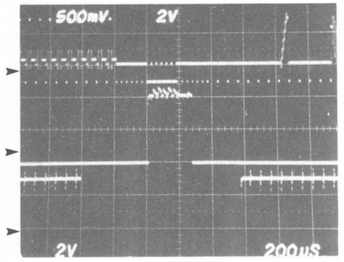
PWA 3 PIN 57
VERTICAL (+)
(FROM TAPE VCO)

WF21

PWA 3 PIN 55
VERTICAL INHIBIT
(–) (TAPE VCO)

WF22

TRIG: PIN 58



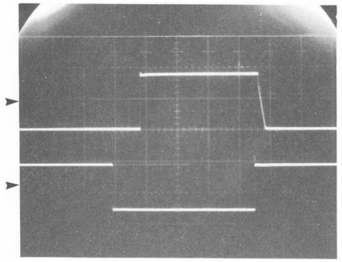
TP15
SECOND SYNC
SLICER

WF24

TP9
RAMP DELAYED
SYNC

WF25

TRIG: TP15

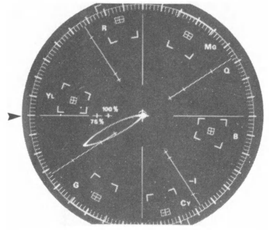


N

PIN 67/68

WF26

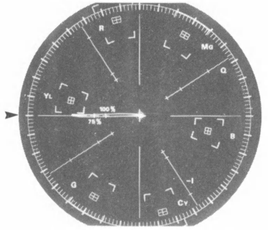
TRIG: EXT ON
REF VIDEO

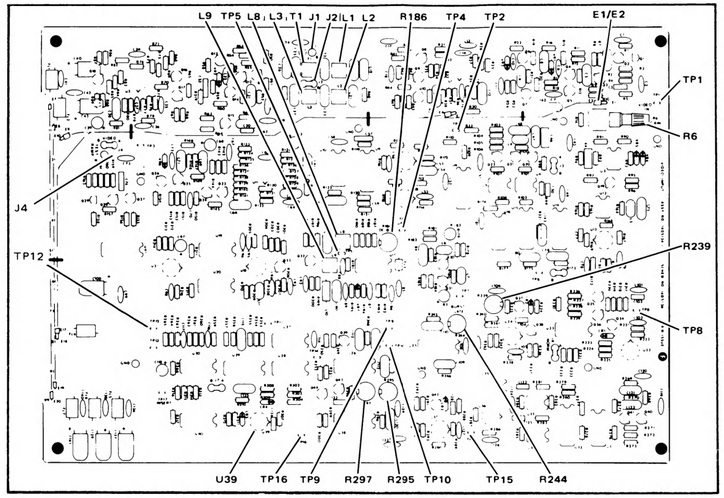


N

COMPARE
WITH WF26

WF27





PWA 3 Component Locator

PWA 3 Jumpers

JUMPER	POSITION – FUNCTION	
J1	Removed A–B	Normal Low-pass filter alignment
J2	A–B Removed	Normal Low-pass filter alignment
J3	A–B Removed	Normal Defeats clamp
J4	A–B B–C	Normal Test ramp
J5	A–B Removed	Normal Defeats noise detector
J6	A–B Removed	Normal Defeats vertical inhibit
J7	A–B Removed	Normal mute Defeats video mute

PWA 3 Adjustable Components

COMPONENT	FUNCTION
L1	Low-pass filter alignment
L2	Low-pass filter alignment
L3	Low-pass filter alignment
L8	Burst filter
L9	Burst filter
R6	Video in gain
R186	Burst amplifier balance
R239	Sync delay
R244	Burst gate
R295	Search servo recovery
R297	Search color detector
T1	Low-pass filter alignment

PWA 3 Test Points

TEST POINT	FUNCTION
TP1	Video input
TP2	X2 video
TP3	Direct/processed video
TP4	Burst gates
TP5	Burst
TP6	Noise gate
TP7	Chroma
TP8	Inverted low-pass video
TP9	Delayed stripped sync
TP10	Diff. stripped sync
TP11	H-rate pulse
TP12	5.4V voltage divider
TP13	H-rate analog
TP14	H-rate pulse
TP15	Stripped sync
TP16	H-rate pulse
TP17	A/D reference insert

SECTION 4

A/D CONVERTER

DESCRIPTION AND MAINTENANCE

4-1. INTRODUCTION

Refer to the following documents in the *Parts Lists and Schematics* manual:

ASSEMBLY No. 1409108

SCHEMATIC No. 1409149

Numbered data sheets (REFERENCE 1, 2, 3 . . . *n*) to which PWA descriptions and maintenance procedures refer are located at the end of this section as follows:

Detailed Block Diagram – REFERENCE 1

Waveforms – REFERENCE 2

Maintenance Data – REFERENCE 2

4-2. DESCRIPTION

The video signal from the Video Input PWA 3 is converted to digital form in the A/D Converter PWA.

Amplitude of the video signal is sampled at three times the subcarrier rate (3 Fsc or 93 ns) and converted to an eight-bit binary number for each sampling period. Thus, one cycle of subcarrier is defined by three samples. The analog video signal is represented in digital form at the output of the A/D Converter as a serial train of binary 8-bit words. Each word can range from 0000 0000 to 1111 1111 (–30 units to 139 IRE units) and represents any of 256 values. The conversion is shown with the test ramp in waveforms 5 through 12 in REFERENCE 2.

Note the A/D reference insert on the sync tip in Waveform 1(A). The A/D reference insert is added in the Video Input PWA to establish a fixed, consistent sync tip insert level within the TBC. Video from the Video Input PWA for 100% saturated color bars is nominally 2 volts and is buffered by a clamp feedback amplifier in the A/D Converter which clamps the sync tip reference to –2 volts. This establishes the quantization reference level of the video to the A/D converter LSI integrated circuit, U6.

The quantization range is shown in Figure 4-1 which gives the relationship between the 256 quantizing levels, peak-to-peak voltage to the A/D converter IC, and equivalent IRE unit measure. The 0–256 bit range corresponds to a –30 to +139.3 IRE level. The clamp amplifier sets the 100% saturated yellow/cyan bar peak at –0.021 volts. This leaves a 2-1/2 quantizing level guard band for best signal-to-noise at peak 100% video level.

A/D conversion is performed by a single integrated circuit which uses a 1-bit pipeline delay technique. A sample is taken (comparators are latched) approximately 10 ns after the rising edge of the convert signal. This delay may vary by a few nanoseconds, but the short-term uncertainty (jitter) in strobe delay is less than 30 picoseconds. The 255 to 8 encoding is performed on the falling edge of the convert signal, and the result is transferred to the output latches on the next rising edge. The outputs require a minimum time to begin changing to the new result. This permits the preceding result to be read on the same rising edge, that is, read data N while acquiring sample N + 2. All timing specifications are with respect to TTL threshold crossing (1.5V). Quantizing levels within the A/D converter are 7.8431 mV per step from 0 to 2 volts.

The A/D converter integrated circuit, U6, is a large-scale integrated (LSI) device in a 64-pin dual in-line package. It is an 8-bit fully-parallel

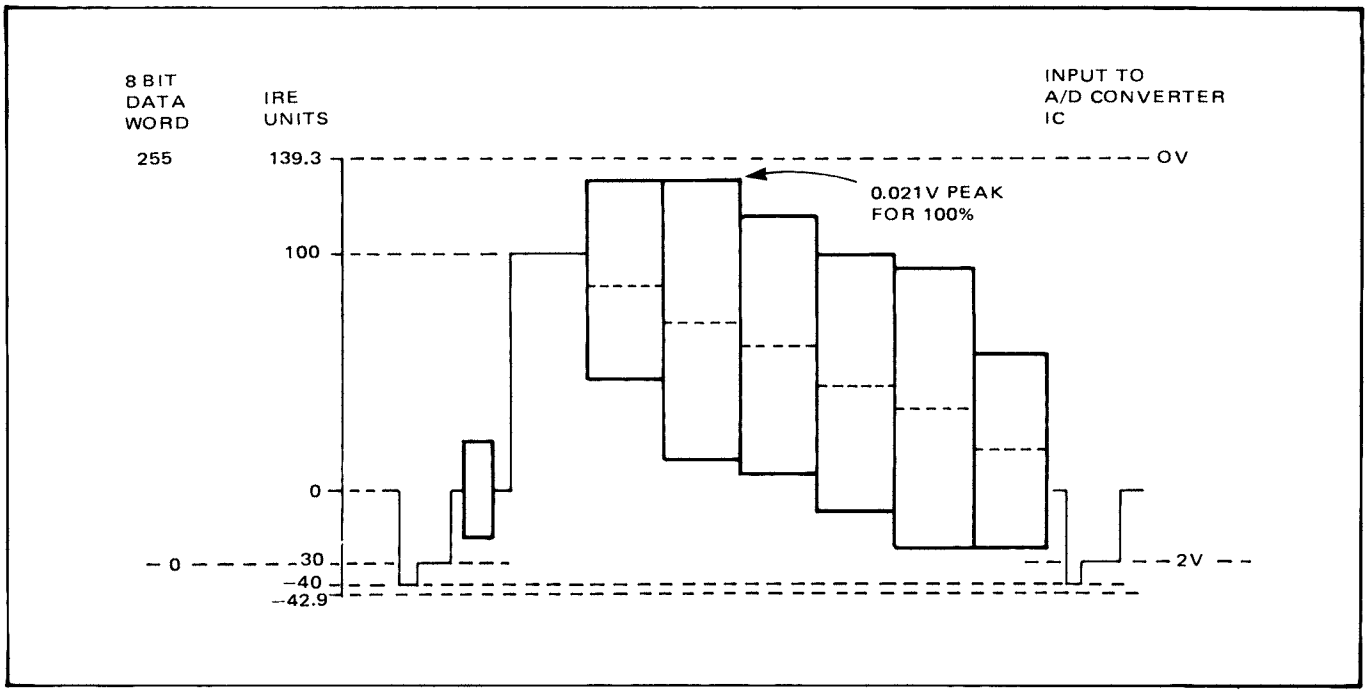


Figure 4-1. A/D Converter Level Definitions

(flash) A/D converter capable of digitizing an analog signal at 3 X subcarrier frequency (3 Fsc). A single convert signal (clock) controls the unit operation, which consists of 255 sampling comparators, combining logic and full-scale step input register. Recovery from a full-scale step input occurs within 20 ns. The digital output is in binary code.

Sampling time is controlled by a 10.7-MHz clock which is phase-locked to the leading edge of the incoming tape H-sync pulse. The phase-locked clock has its origin in a 10.7-MHz 3 X subcarrier oscillator on the Tape H Comparator PWA 5.

The 8-bit binary value in the A/D converter device is clocked into an 8-bit output register on the A/D Converter PWA by the rising edge of the common 3-Fsc clock. Thus, total pipeline delay of the A/D Converter PWA is two bits. The signal from the PWA output register is routed to the Serial-to-Parallel Converter PWA 8.

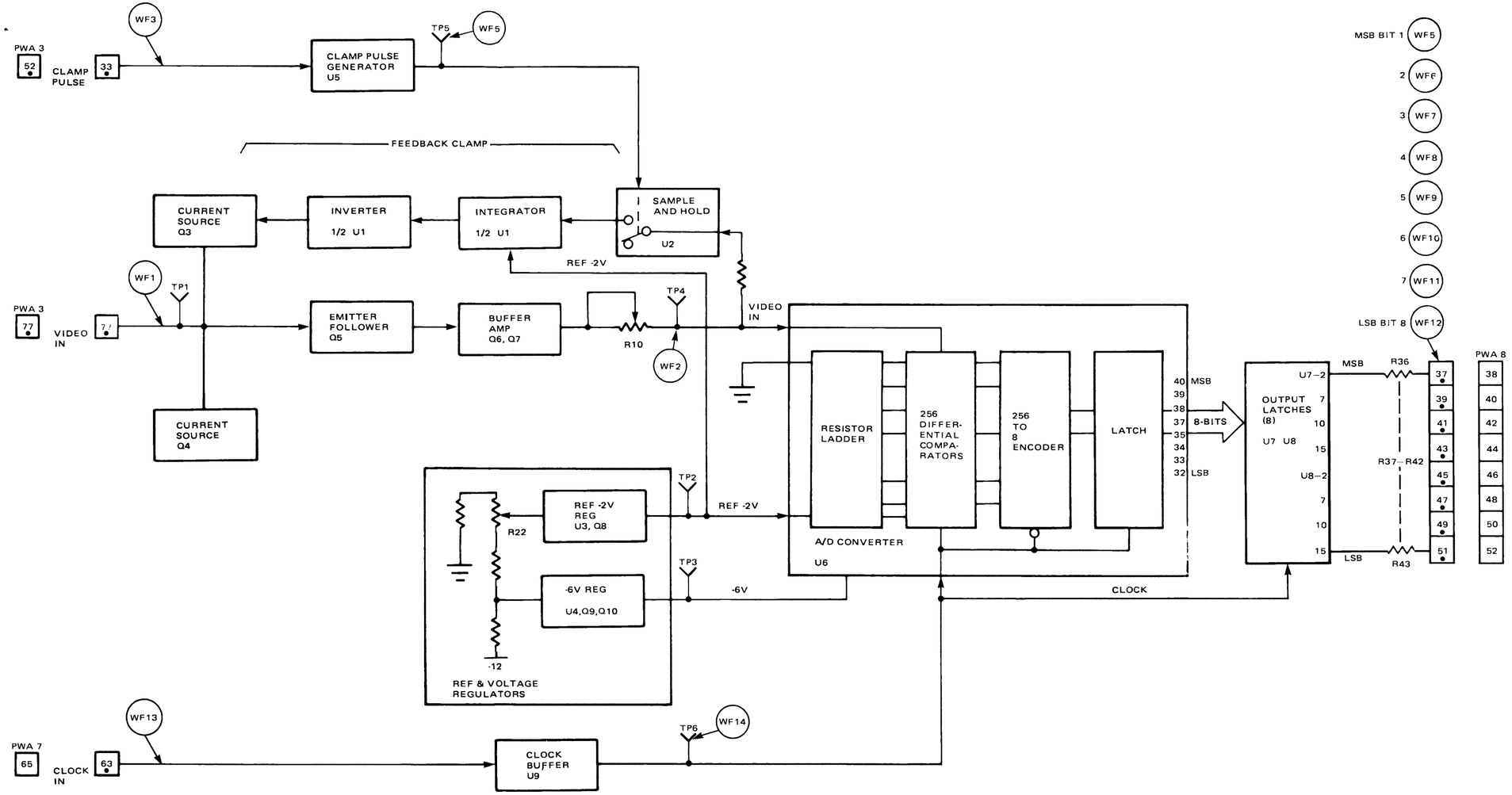
4-3. A/D CONVERTER MAINTENANCE

See REFERENCE 2 in this section for component locator diagram and jumper/test point/adjustable component summaries.

Review the *System Alignment Guide* (Table 3-2) and *Tape/Reference Test Loop* discussion (Paragraph 3-5) in the *System Maintenance* section (Part I) for a general understanding of the context for maintenance on the A/D Converter.

Consult reference waveforms and interconnect data on the simplified schematic to confirm normal operation of the A/D Converter and interactive functions between it and other PWA's.

There are two controls on the A/D Converter PWA, but neither R10 (video damping) nor R22 (converter gain) should require adjustment except that necessitated by component failure. Converter gain control R22 sets up quantizing increments. A 2.000-volt dc value at TP2 is correct for the unity gain levels on the Video Input PWA. Video damping control R22 affects low-end frequency response.



Detailed Block Diagram,
A/D Converter PWA 4
REFERENCE 1

A

PIN 77/78
VIDEO IN (TP1)

WF1

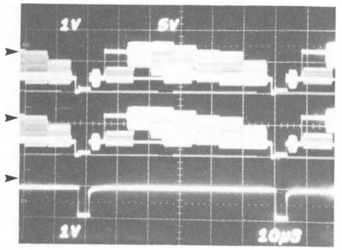
TP4
A/D CONVERTER
CHIP VIDEO IN

WF2

PIN 33/34
CLAMP PULSE

WF3

TRIG: PIN 33



B

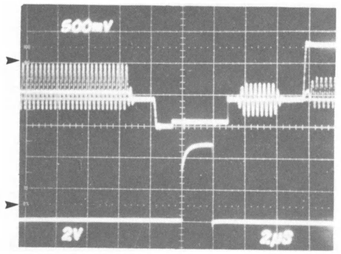
TP4

WF2

TP5
SAMPLE PULSE

WF4

TRIG: PIN 33



C

TP4

WF2

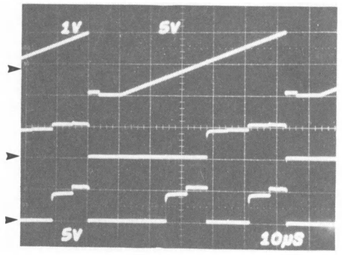
PIN 37/38
(MSB)

WF5

PIN 39/40
BIT 2

WF6

SCOPE EXT. TRIG: PIN 33
TEST RAMP INSERTED
A3 J4 TO B TO C POSITION



D

TP4

WF2

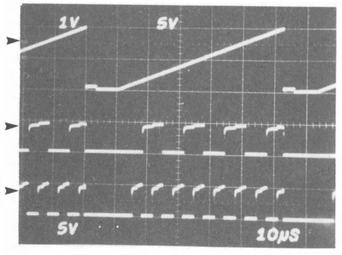
PIN 41/42
BIT 3

WF7

PIN 43/44
BIT 4

WF8

TRIG: TP5 TEST RAMP IN



TP4

PIN 45/46
BIT 5

PIN 47/48
BIT 6

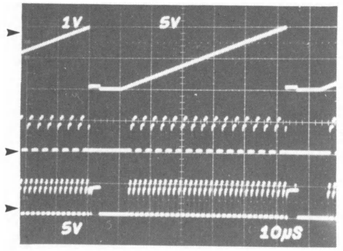
SCOPE EXT. TRIG:
TP5 TEST RAMP IN

E

WF2

WF9

WF10



TP4

PIN 49/50
BIT 7

PIN 51/52
(LSB) BIT 8

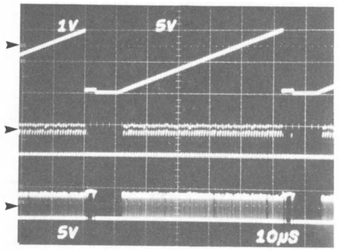
TRIG: TP5
RAMP IN

F

WF2

WF11

WF12



TP4

PIN 37/38
(MSB)

PIN 51/52
(LSB)

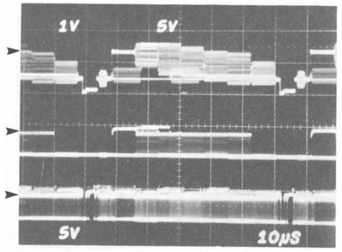
TRIG: TP5

G

WF2

WF5

WF12



PIN 63/64
CLOCK

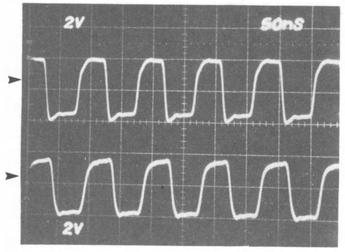
TP6
CLOCK BUFFERED

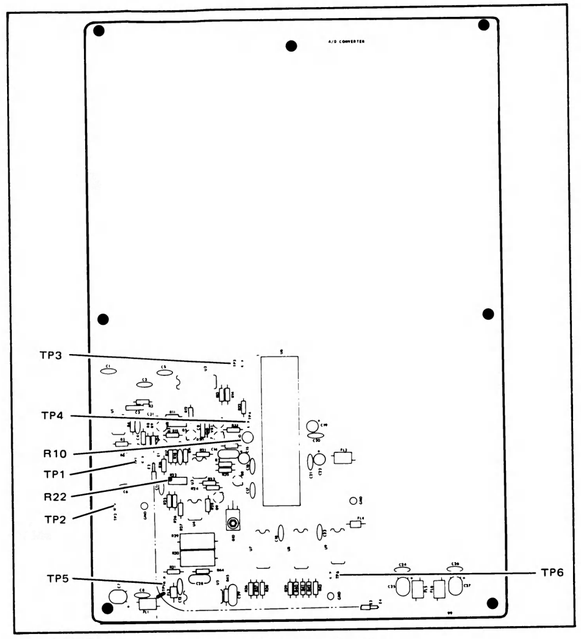
TRIG: PIN 63/64

H

WF13

WF14





PWA 4 Component Locator

PWA 4 Test Points

TEST POINT	FUNCTION
TP1	Video in
TP2	-2.00 Vdc
TP3	-6.00 Vdc
TP4	Converter video
TP5	Sample pulse
TP6	Clock

PWA 4 Adjustable Components

COMPONENT	FUNCTION
R10	Video damping
R22	Converter gain

Waveforms, Test Points, Adjustable Components, Component Locator, A/D Converter PWA 4
REFERENCE 2

SECTION 5

TAPE H COMPARATOR
DESCRIPTION AND MAINTENANCE

5-1. INTRODUCTION

Refer to the following documents in the *Parts Lists and Schematics* manual:

ASSEMBLY No. 1409104

SCHEMATIC No. 1409106

Numbered data sheets (REFERENCE 1, 2, 3 . . . *n*) to which PWA descriptions and maintenance procedures refer are located at the end of this section as follows:

Overall Block Diagram – REFERENCE 1

PWA 5/PWA 6 Signal Relationships – REFERENCE 2

Simplified Schematic – REFERENCE 3, 4

Waveforms – REFERENCE 5, 6, 7

Maintenance Data – REFERENCE 7

TAPE H COMPARATOR
PWA 5 FUNCTION SUMMARY

- Works in conjunction with the Tape VCO PWA to synchronize the TBC's memory write control signals to the off-tape H-sync pulses.
- Compares phase of off-tape H-sync pulses with phase of sync pulses produced by VCO on Tape VCO PWA.
- Produces a line-by-line velocity error voltage and provides it to the Velocity Compensator option.
- Provides sync-coherent subcarrier to the Color Processor PWA.

5-2. DESCRIPTION

The function of the Tape H Comparator PWA 5 is to accept synchronizing signals from the Tape VCO PWA 6 and Video Input PWA 3 and to process them to produce sync signals for the TBC system that are phase-locked to a selected color burst crossing (Fsc). An exception is in heterodyne mode where Tape H Sync from the Video Input PWA 3 is selected by the MODE switch (TBC front panel) which operates the Tape VCO sync select in the Tape VCO PWA. See REFERENCE 2, PWA 6 and PWA 7 Signal Relationship, Simplified Block diagram.

The Tape H Comparator and Tape VCO PWA's are functionally one large interdependent circuit. In normal mode, with color present, signal processing begins on the Tape H Comparator with phase comparison of the timing relationship between the leading edge of a delayed Tape H Sync and a selected burst crossing from the Video Input PWA. Horizontal sync of Tape VCO is derived from the selected burst crossing from the Tape H Comparator. The 6-Fsc oscillator is phase-locked to this H-sync and thus to the selected burst crossing.

With the exception of 6 Fsc, signals from the Tape VCO are derived from the 6 Fsc divide-by-1365 counter decode. Thus, signals from Tape VCO are phase-locked to selected burst crossing. However, these signals contain VCO errors which will be removed by the Tape H Comparator PWA.

The normal 6-Fsc oscillator has a long time constant of approximately 16 lines. Circuits on the Tape H Comparator, centered around the control logic and the error voltage generator, provide a faster time constant phase correction of synchronizing signals from the Tape H Comparator to the TBC-2 system. Signals from the

Tape H Comparator to the Tape VCO are comparator timing and 7.8 kHz. Signals from the Tape VCO to the Tape H Comparator are 6 Fsc, 1/2-line, qualified H-pulse, frequency error, and VCO write pulse. Tape VCO 6 Fsc generates VCO 3 Fsc via a divide-by-2 counter. VCO 3 Fsc is applied to a divide-by-3 counter to produce VCO Fsc. VCO 6 Fsc and VCO 3 Fsc drive a two-stage phase shifter which is modulated by the error voltage generator. This provides line-by-line correction of the Tape VCO 3 Fsc output and write pulse output timing. These signals, with 7.8 kHz, are used by the Memory Control PWA 7 to control the memory write function at tape rate.

VCO Fsc is sampled and summed against the voltage from the error voltage generator. The resultant line error output signal is used by the velocity compensator option on the Parallel-to-Serial Converter PWA 13 in the memory read function to correct for timing errors introduced into the video signal during the horizontal line due to velocity errors.

In slow-motion operation the frequency error signal from the Tape VCO modulates the burst phase detector and thereby the Tape H Comparator output signals to correct for the phase shift of 3.58 MHz in the burst filter of the Video Input PWA. (In slow-motion, burst is 3.58 MHz −1%.)

5-3. Burst Crossing to Tape H-Sync Phase Relationship (See Waveforms G, H, I)

To preserve the integrity of the H-sync-to-chroma-phase relationship, the video signal is tested on a line-by-line basis to determine if a burst is present. If the result is positive, the burst crossing selector is enabled. If burst is not present, the associated sync/burst phase circuitry is inoperative for that line. When enabled, the burst crossing selector is clocked to a reset condition by the selected burst crossing. Therefore, the trailing edge of the output pulse represents the selected burst crossing to the sync/burst phase circuitry. Because the chroma subcarrier is an odd multiple of one-half the horizontal rate, the phase of chroma relative to H-sync shifts 180 degrees on alternate lines; therefore, the timing of the delayed tape H-sync on the Tape H Comparator PWA is shifted by 140 nanoseconds on alternate lines by the 7.8-kHz signal (1/2 line divided-by-2).

$$Fsc = \frac{455}{2} \times 15.73426\ kHz = 3.579545\ MHz$$

1/2 cycle of Fsc = 140 ns

one cycle of Fsc = 279 ns = 227.5 cycles of Fsc/line

(See Figure 5-1, Selected Burst Crossing Timing Relationship.) The delayed tape H-sync (shifted 140 degrees, alternate lines) is further delayed so that the leading edge will occur at a zero crossing during a negative-going transition of the selected color burst cycle. This pulse is used to enable the burst crossing voltage comparator. The next following positive zero crossing of burst clocks the selector reset and cancels the enable. The selected burst crossing from the burst crossing comparator is used in three ways: (1) to reference the comparator timing output of the Tape H Comparator PWA to the burst crossing, (2) as an input to the sync/burst crossing comparator to maintain a constant sync/burst crossing time relationship, and (3) as an input to the slow-motion burst phase correction circuit.

The Q output of the 7.8-kHz flip-flop is AND'ed with selected burst crossing in one gate. The $\overline{Q}$ output is AND'ed with selected burst crossing in another gate. When $\overline{Q}$ is high, the signal is delayed by 140 nanoseconds and applied to a one-shot which generates the comparator timing pulse. When $\overline{Q}$ is high (next line) the signal is applied directly to the comparator timing one-shot. Thus, the 140 nanosecond phase shift on alternate lines for the burst crossing selector is removed and the comparator timing (H-sync) to the Tape VCO PWA occurs at a positive transition of Fsc on one line and at a negative transition on the next line.

(See waveforms M, E, F.) The sync/burst crossing phase-comparator circuits with the associated ±225-degree limit detector modulate the burst phase vernier to maintain the sync/burst timing relationship. Delayed tape H from the alternate line burst-phase-select one-shot dumps the charge on C36, setting the input of the buffer amplifier

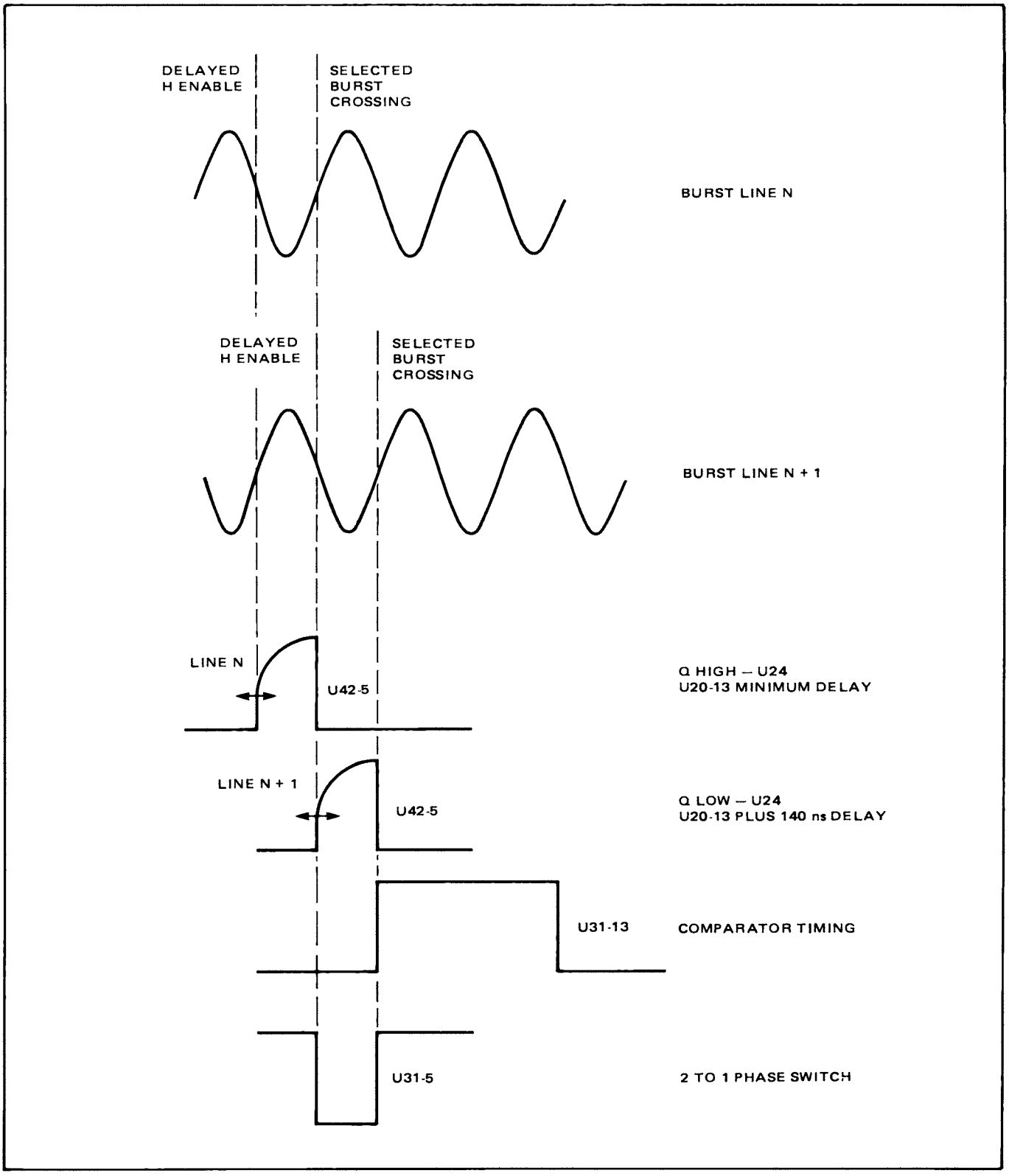


Figure 5-1. Selected Burst Crossing Timing Relationship

to a reference level of –5.2 volts. The burst crossing selector enable starts a ramp charge on C36. The selected burst crossing stops the ramp. The voltage value achieved is proportionate to the time relationship between the two signals. The burst crossing selector pulse operates the sample-and-hold circuit. The output of the sample-and-hold buffer is used two ways: it modulates the pulse width of the burst phase vernier one-shot and it is applied to two limit detectors. The ± 225-degree limit detector operates a reset to center range switch which dumps the charge on sample-and-hold capacitor C104 if the error signal is outside the reference limits. This condition can occur when edits are made in which color burst on the edited material is too far out of phase, in which case the dump to center is made and a new burst crossing is selected. When the burst phase is within ± 40 degrees the edit ready light on the control panel is on.

(See waveform M.) The selected burst crossing is also applied as an input to the burst phase correction circuits. The frequency error signal is a measure of the long-term H-rate error from the tape. This is applied to one input of a voltage comparator. The other input is a ramp initiated by burst crossing. A programmable counter U11, started by burst crossing, resets the enable of the comparator at the end of its count.

The resultant pulse out of the comparator is a phase correction for burst crossing when tape speed is other than normal. The corrected burst crossing starts the action in the control logic. An entry flip-flop is clocked set with burst crossing and reset two 6-Fsc pulses later. After the first of these 6-Fsc pulses, the load data is removed from the programmable counter. After the second 6-Fsc pulse, a two-stage shift register resets the entry flip-flop and holds the load data high until the carry from the programmable counter, clocked by 6 Fsc, resets the shift register. The carry also latches data from the divide-by-two and divide-by-three (3 Fsc, Fsc) counters. After a few nanoseconds of gate phase delay, the carry resets the 3Fsc and Fsc counters to zero and the count starts over. The number stored in the latch is a measure of the "length" of the previous line as predicted by the VCO 6-Fsc oscillator. This oscillator has a time constant of approximately 16 lines and is therefore capable of only relatively long-term corrections. The number stored in the latch is converted to an analog value by a D/A converter.

The pulse developed by the entry flip-flop will actually be three 6-Fsc pulses in length if there is no tape error and the 6- Fsc oscillator is phase-locked to burst crossing. If an error exists, the pulse will be decreased in direct proportion to the phase error. The pulse is used to initiate and time out a ramp generator in the phase error voltage generator. The voltage developed by the ramp at the termination of the pulse is stored in a sample-and-hold circuit. This error voltage is a line-by-line measure of velocity error. It is summed with the value from the D/A converter in a summing amplifier and sent to the Parallel-to-Serial Converter PWA to provide a line-by-line error value for the velocity compensation option to operate on.

(See waveforms M, N, O and P, Q, R.) The output of the phase error voltage generator is also used to modulate the two-stage 3-Fsc generator. Modulated 3 Fsc from the Tape H Comparator PWA is used by the Memory Control PWA to sample the video signal. The sample must be made at a rate which is consistent with line-to-line velocity errors. Although the chroma may be in error relative to the station master subcarrier, it must be sampled with the velocity errors intact so that it can be clocked out of memory at the correct rate to achieve time-base correction. The 3 Fsc derived from the VCO 6 Fsc is phase-modulated by the line-by-line velocity error signal to produce a clock which is phase-locked to H-sync and burst at a rate which reflects actual tape rate.

The VCO write pulse reclock circuit does two things: it provides a measure of the phase relationship of VCO write pulse to the next following VCO Fsc pulse, and reclocks the resulting pulse with the modulated 3 Fsc. The reclocked VCO write pulse is one input of the encode Fsc phase shift circuits which will be discussed later.

5-4. Programmable Counter

Encoded inputs to the programmable counter are as follows:

	COLOR NORMAL	MONO NORMAL	HET COLOR	HET MONO
Bit 1	1	1 and 0	1	1 and 0
Bit 2	1	1	1	1
Bit 4	0	0 and 1	0	0 and 1
Bit 8	0	1	1	1
Count	12	4 or 1	6	4 or 1

The 7.8-kHz signal gated in by MONO mode results in a difference of three 6-Fsc pulses from one line to the next. The length of time the programmable counter is permitted to operate will have an effect on the number stored in the Fsc counter latch and ultimately on the voltage developed by the D/A.

5-5. Tape H Comparator PWA 6 Encode Fsc Circuit

The encode Fsc circuit is used, in heterodyne mode, to phase-lock Fsc to the VCO write pulse. The encode Fsc is reshaped as a sine-wave in the color processor and sent to the heterodyne VTR to be used to remodulate the tape chrominance signal (sync-coherent 3.58 MHz out).

In heterodyne mode, H-sync circuits on the Tape VCO PWA are driven by tape H-sync from the Video Input PWA. This signal is derived from off-tape video from the heterodyne VTR. The 6-Fsc oscillator on the Tape VCO PWA is phase-locked to the selected H-sync.

The 6-Fsc oscillator is applied to a divide-by-1365 counter. One of the decodes of the counter generates the VCO write pulse. The encode Fsc is phase-locked to the VCO write pulse by the entire loop and therefore locked to the tape H-sync.

In the Color Processor PWA the 3.58-MHz crystal oscillator is phase-locked to the same sync-coherent 3.58 MHz used by the heterodyne VTR remodulation. The output of the crystal oscillator is used to demodulate the B–Y and R–Y signals from the heterodyne VTR chrominance signal. The demodulated B–Y and R–Y signals are then encoded with tape-sync-coherent 3.58 MHz. What was an asynchronous chrominance signal from the heterodyne VTR is now sent to the Video Input PWA with chrominance phase-locked to tape H-sync.

The encode Fsc circuit consists of a divide-by-6 counter clocked by 6 Fsc and a three-stage counter circuit used as a digital phase-lock for the divide-by-6 counter.

(See Figure 5-2 Encode Circuit Block Diagram.) The VCO write pulse clocks a flip-flop which is reset by the following Fsc pulse from a divide-by-6 counter clocked by VCO 6 Fsc. The result is a pulse width which is proportionate to the time between the two events. This reclocked VCO write pulse enables the first stage of the digital phase lock. The counter is clocked by 6 Fsc. The load signal, inhibiting the counter, is removed just prior to the VCO write pulse time by a delayed H-pulse. If the counter result is greater than five at the end of the enable period, the second stage counter will decrement one count. If the result is less than four, the second stage will increment one count. The binary output of the second stage programs the third stage, the third stage is loaded by its carry output which also resets the divide-by-6 counter. The third stage is therefore a variable delay to reset the divide-by-6 counter, thus changing the phase relationship of encoded Fsc and VCO write pulse. The reset signal is AND'ed with 7.8 kHz and as a result will be applied to the divide-by-6 counter only on every other line. In addition, in the case of a serious phase error, because the second stage counter is changed only one count per alternate line, many lines may be needed to complete the phase shift until the count of the first stage is either 4 or 5, the target window.

(See Figure 5-3, Encode Fsc Feedback Loop Block Diagram.) From the preceding paragraphs it can be seen that the circuits on the Tape H Comparator, Color Processor, Video Input, Tape VCO, and the heterodyne VTR are used as one long servo loop to maintain the sync-to-burst relationship.

5-6. TAPE H COMPARATOR MAINTENANCE

See REFERENCE 5, 6, and 7 in this section for component locator diagram, jumper/test-point/adjustable component summaries, and waveforms called out in these procedures.

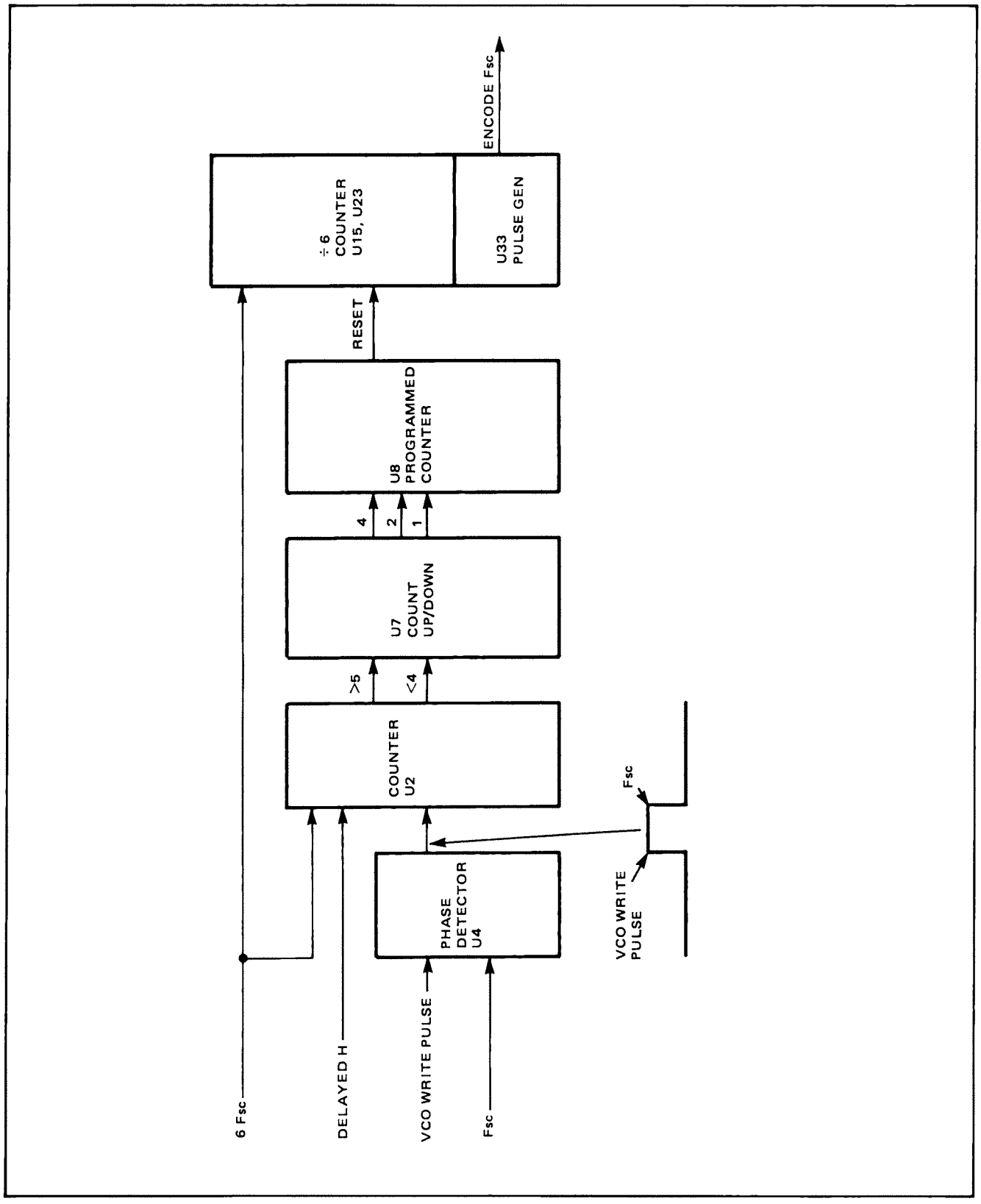


Figure 5-2. Encode Fsc Circuit Block Diagram

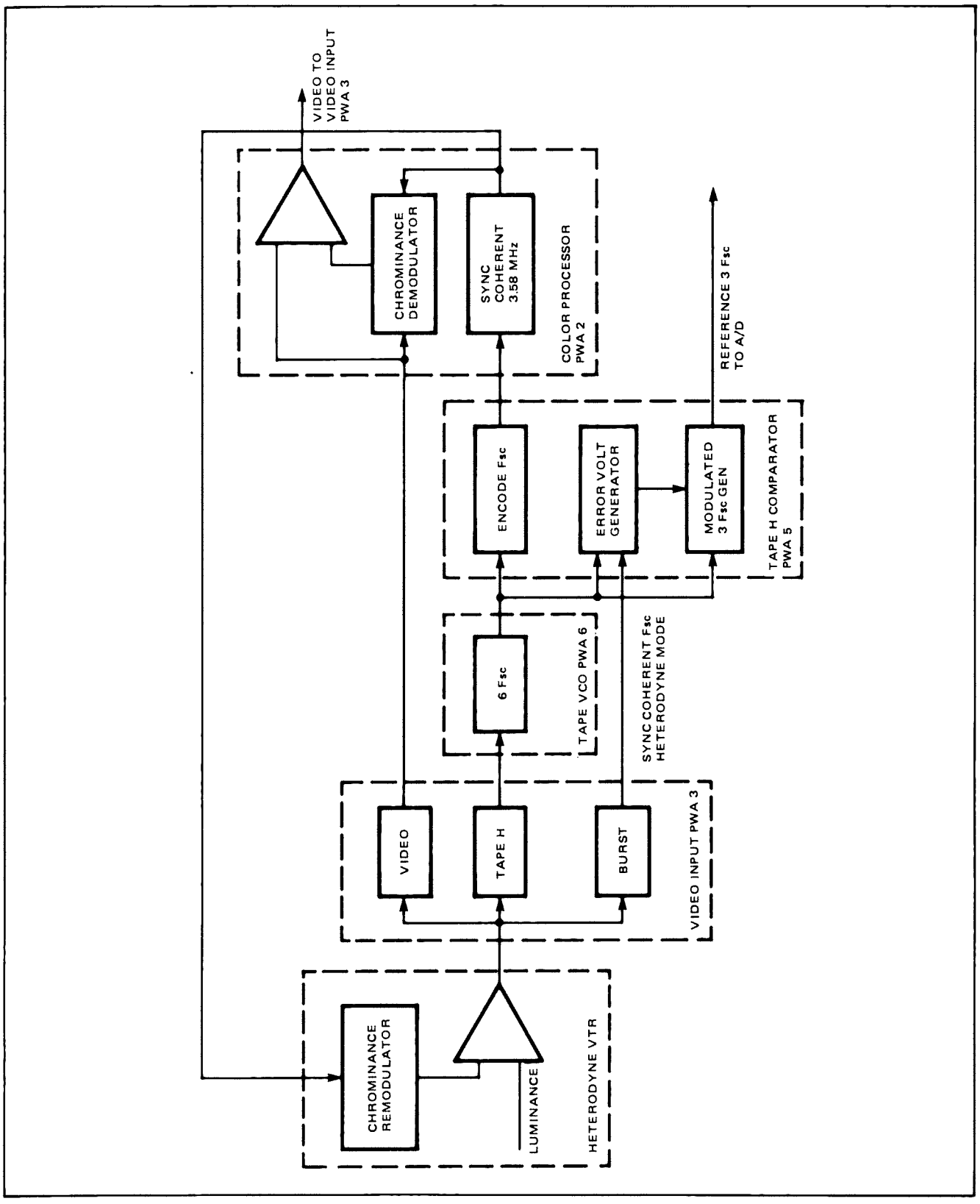


Figure 5-3. Heterodyne 2-Wire Connector

Before undertaking any adjustments to the Tape H Comparator, review the *System Alignment Guide* (Table 3-2) and the *Tape/Reference Test Loop* discussion (Paragraph 3-5) in the *System Maintenance* section (Part I) for a general understanding of the scope of these field adjustments.

Consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the Tape H Comparator and interactive functions between it and other PWA's before making any adjustments.

The Tape H Comparator and the Tape VCO are uniquely interactive and any adjustment to the Tape H PWA should be preceded by checks at the Tape VCO that insure the VCO and frequency error discriminator circuits are operating normally.

5-7. Tape H Comparator Alignment

1. Use tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN. For consistently color-framed edits it is imperative that the signal generator burst/sync phase be set for RS170A (burst negative-going zero crossing coincident with the 50% point of H-sync leading edge on Field 1) or standard reference of the facility.

2. Burst crossing calibration:

   a. With power off extend Tape H Comparator.

   b. Set R1 (burst/sync phase) to center of its range.

   c. Connect oscilloscope —

      Channel 1: TP10 (burst crossing sheet)

      Channel 2: PWA pin 69

      Trigger: PWA pin 25

      Use delayed sweep and chop mode to display burst and two pulses as shown in WF4/29(V).

   d. Adjust R117 (burst crossing) so that the negative edge of the later of the two pulses occurs just before peak of burst.

   e. Carefully readjust R117 until EDIT READY light on control panel is illuminated.

   f. Adjust R1, burst/sync phase, counter-clockwise until the EDIT READY light is extinguished. Note position of R1.

   g. Adjust R1 clockwise until EDIT READY light comes back on and then goes out again. Note position of R1.

   h. Set R1 midway between the two points noted above. Verify that EDIT READY light is illuminated in this center position.

   i. Verify a dc level of +3.2 (±0.3) volts at U56-6 with EDIT READY on.

3. Tape H-Sync-to-Video Timing: If the Tape H Comparator, Tape VCO, or Memory Control PWA's are repaired or the TBC is phased to a nonstandard reference, H-sync timing may require readjustment.

   a. Use tape/reference test loop setup with a 75% split field color-bar signal at standard level and sync/burst phase (or nonstandard facility reference) connected to TAPE VIDEO IN.

   b. Switch TBC mode to NORMAL.

   c. With power off remove Video Input PWA and connect a clip lead to TP12 long enough to reach any convenient grounding point after PWA is reinserted into cage.

   d. With power off extend Tape VCO PWA.

   e. Switch power on and verify that EDIT READY and Sync Generator REFERENCE SYNC/BURST CALIBRATION indicators are on. Refer to tape H comparator and sync generator alignment procedures if indicators are not on.

   f. Connect an oscilloscope to VIDEO OUT 1 and using delayed sweep, line up leading edge of the white bar on the center graticule. Use sufficient sensitivity to see any horizontal shift within a subcarrier cycle. This will be the reference point for the next steps.

g. Ground TP12-connected clip lead and note any shift of video.

h. Adjust R53 (H-sync phasing) to reposition white bar edge on the center graticule.

i. Alternately open and short clip lead to ground while adjusting R53 for minimum horizontal shift.

j. With power off remove clip lead from TP12 and return both PWA's to the cage.

k. Turn power on and switch TBC between NORMAL and BYPASS. Note any shift in picture position.

l. If there is a shift in picture position turn the thumbwheel horizontal phasing switch on Memory Control PWA to a position that minimizes horizontal shift.

m. Switch TBC power on and off several times and verify that picture position remains the same.

4. Comparator timing adjustment:

   a. Connect oscilloscope –

      Channel 1: U25-12 (PWA pin 26, comparator timing)

      Trigger: U31-1

      Use delayed sweep to display pulse shown in WF30(W).

   b. Set R2 to center of its range. The final setting for R2 will be made with write pulse reclock phase adjustment below.

   c. Adjust R128 (phase balance) minimum jitter of positive edge of pulse. The top trace of WF30(W) shows correct adjustment. The effect may also be seen with a vectorscope on video output where R128 is adjusted for minimum jitter of blue vector.

5. Phase modulator offset-search adjustment:

   a. Connect oscilloscope triggered on line or a DVM for a dc measurement at TP8.

   b. Position jumper J1 to B–C.

   c. Adjust R54 (test phase modulation) for –0.8 Vdc at TP8.

   d. Return J1 to A–B.

      R54 may be set for –0.8 Vdc in a dynamic mode (J1 in A–B) with VPR in shuttle at a speed that shifts picture to monochrome.

6. Tape 3 Fsc symmetry adjustment:

   a. Connect oscilloscope triggered on internal to PWA pin 64 (tape 3 Fsc).

   b. Adjust R180 (clock symmetry) so that slopes of lower 50% of waveform are symmetrical.

7. Write pulse reclock phase adjustment:

   a. Connect oscilloscope –

      Channel 1: TP4 (VCO write pulse)

      Trigger: Signal Generator H Sync

      Use delayed sweep and chop mode to display the two pulses (field 1/2).

   b. Adjust R2 fully clockwise, then counterclockwise until the right-hand pulse is between 130 and 150 nanoseconds at the 50% point as shown in WF31(X). The pulse width will change in 46-μs increments (6 Fsc rate).

8. Heterodyne (and slow motion) encode Fsc symmetry adjustment:

   a. Connect oscilloscope –

      Channel 1: U29-10 (PWA pin 75 – encode Fsc)

      Trigger: Internal

   b. Switch MODE to HET.

   c. Adjust R25 (symmetry) for a symmetrical square wave.

   d. Return MODE to NORMAL.

5-8. Velocity Compensator Line Error Adjustment

The R3/R4 modulator adjustments and the vel comp adjustments on PWA 13 are made at the factory with a highly accurate servo test instrument and should not be adjusted unless the need is well established. This procedure should precede the PWA 13 adjustments. If the velocity compensator option was added later to the TBC it will have been similarly adjusted and only PWA 13 R1 (vernier correction gain) need be adjusted as outlined in the *PWA 13 Alignment* procedures, Paragraph 13-18.

1. With power off remove jumper J2 from P/S Converter PWA 13 and return PWA to its slot. This disables the second-order correction.
2. Make the normal VTR/TBC hookup and monitor VIDEO OUT 1 with the vectorscope. Do not extend the PWA for the R3/R4 adjustment below.
3. Play a recording of 75% color bars.
4. Adjust R3 (phase modulator gain) for a minimum yellow vector dot.
5. Switch velocity compensator on (PWA 13 S1 up).
6. Adjust R4 (velocity balance) for minimum vector dot spread on blue vector.
7. With power off return PWA 13 jumper J2 to A–B.
8. Readjustment of chroma phase (PWA 15 R 146) may be required. Refer to *Sync Generator PWA Adjustment* section.

5-9. Slow/Reverse/Still-Motion Adjustment with the VPR-2B

Adjustment with the VPR here requires a normal VPR/TBC configuration with both units fully operational and properly phased to the system reference (RS170A sync/burst phase or the facility standard reference). It is crucial to maintain normal video from the VPR for this procedure.

1. Verify normal chroma output from the chroma inverter circuits of the Color Processor PWA as outlined in Paragraph 2-9, *Heterodyne/Slow Motion Output.*
2. Connect waveform monitor and vectorscope to VIDEO OUT 1.
3. Make a 10-minute recording of split field color bars (RS170A or facility standard sync/burst phase).
4. With power off extend Tape H Comparator.
5. Connect digital voltmeter to TP12 (dynamic error).
6. While playing back tape adjust R108 (dc offset) for 0.0 (±0.1) volts dc at TP12.
7. Connect DVM to U44 pin 7.
8. Play back tape at normal speed and verify that EDIT READY indicator is on and DVM reads 4.10 (±0.01) at U44-7.
9. At waveform monitor on VIDEO OUT 1 expand (X 25 magnification) rising edge of I and Q signal of the split field and set this edge to a reference point on the graticule (or use the transition between green and cyan bars) for observation of picture shift during next step.
10. Shift VPR to full-speed slow motion (carefully, to avoid losing head-to-tape contact), then to still frame and to full-speed reverse motion and observe the following:

    a. EDIT READY stays on.

    b. No picture shift.

c. U44-7 voltage stays within 4.07 – 4.13 volts.

If any of these conditions are not met the R170 (slow-motion static error) and R157 (slow-motion dynamic error) adjustments in the next steps are indicated.

11. Continue playback and turn VPR speed control to still frame mode (center detent).

12. Verify that R157 is near mid-range and adjust R170 for 4.10 (± 0.1) Vdc at U44-7.

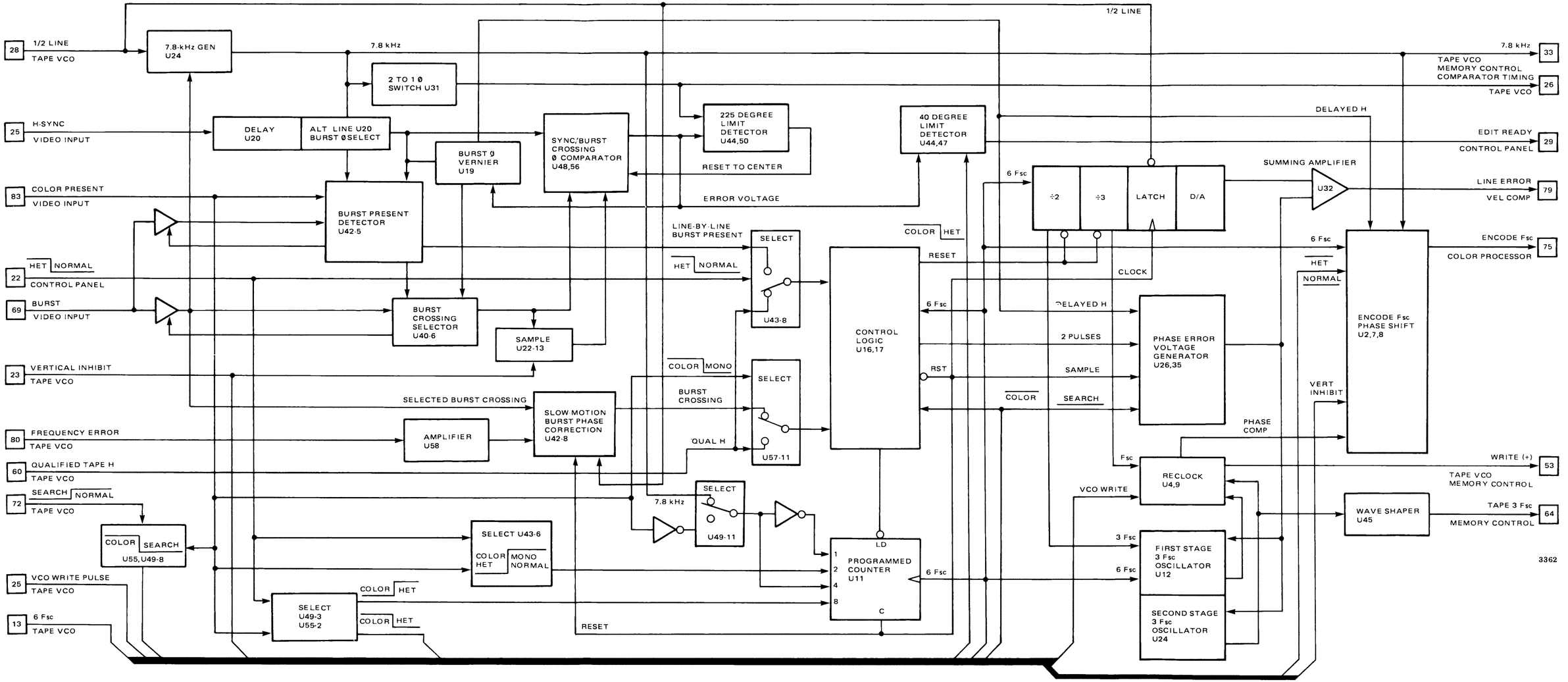
13. Try step 9 again and note voltage at full speed forward and reverse motion. If voltages in step 9 are between 4.07 and 4.13 volts, then go to next step. If not, with VPR in full-speed reverse slow motion, adjust R157 for a voltage at U44-7 midway between voltages noted in previous step. Then repeat steps 9–12 until voltage at U44-7 is between 4.07 and 4.13 volts.

14. Play back VPR in normal speed and note position of vectors on vectorscope.

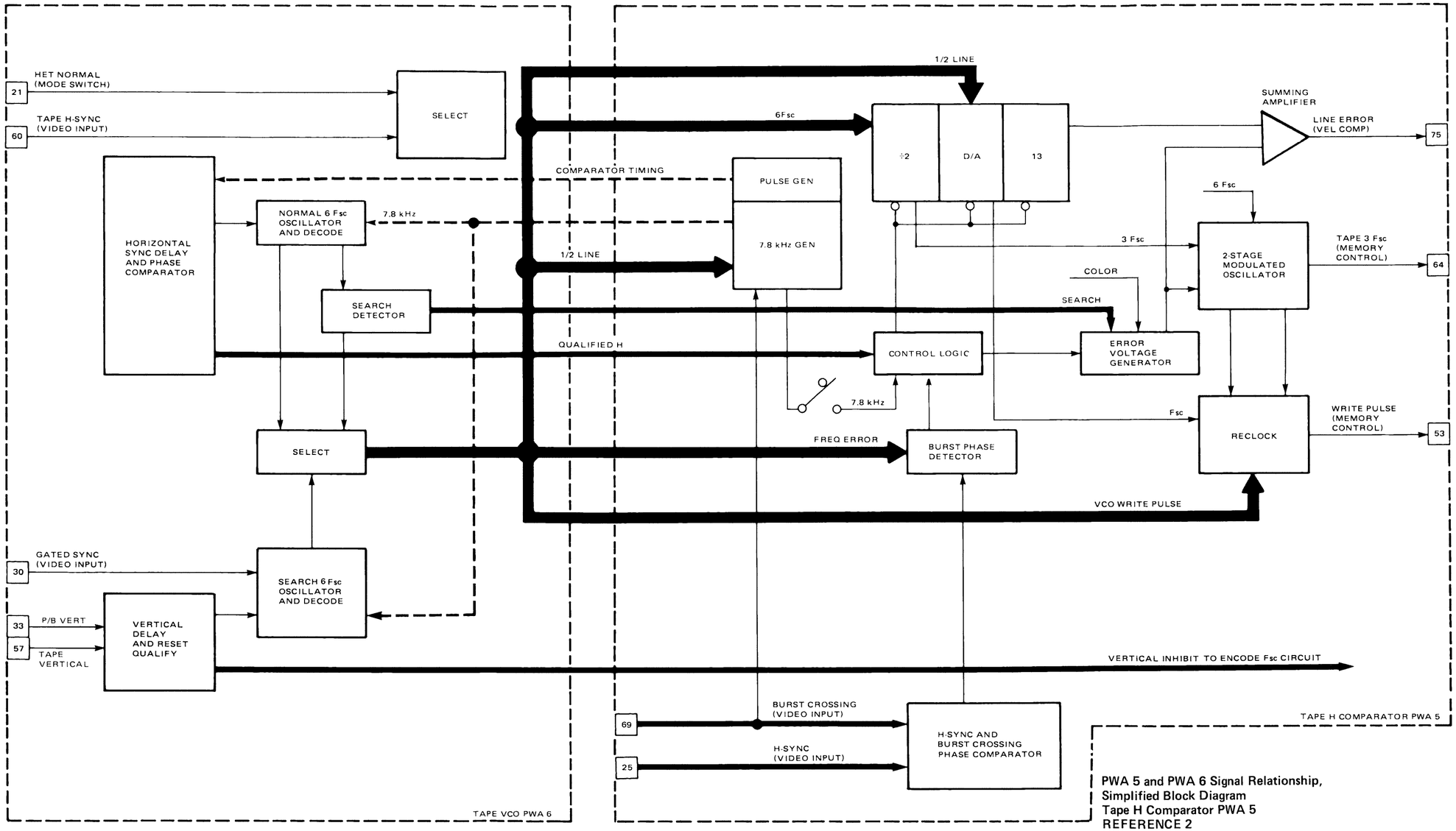
15. Play back VPR in full speed reverse slow motion. Adjust R155 for vectors in same location as in play on vectorscope.

16. Play back VPR in all speeds of slow motion: REVERSE, STILL, and FORWARD. Verify no picture shifts, no vector shifts, clean picture with no break-up, EDIT READY stays on, and colors are correct. Verify with VPR sync head both off and on (VPR-2B PWA number 8).

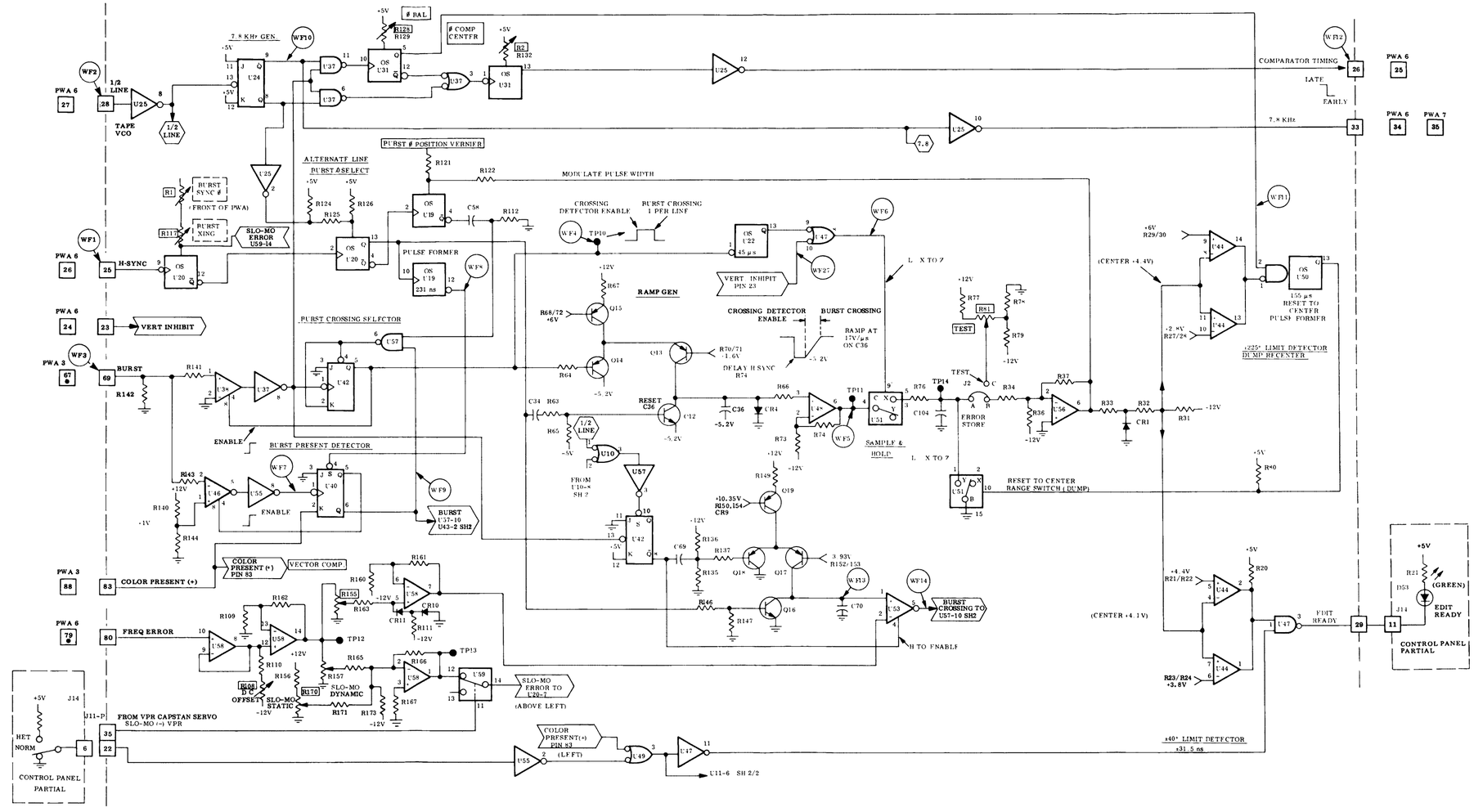
17. With power off return Tape H Comparator to the cage.



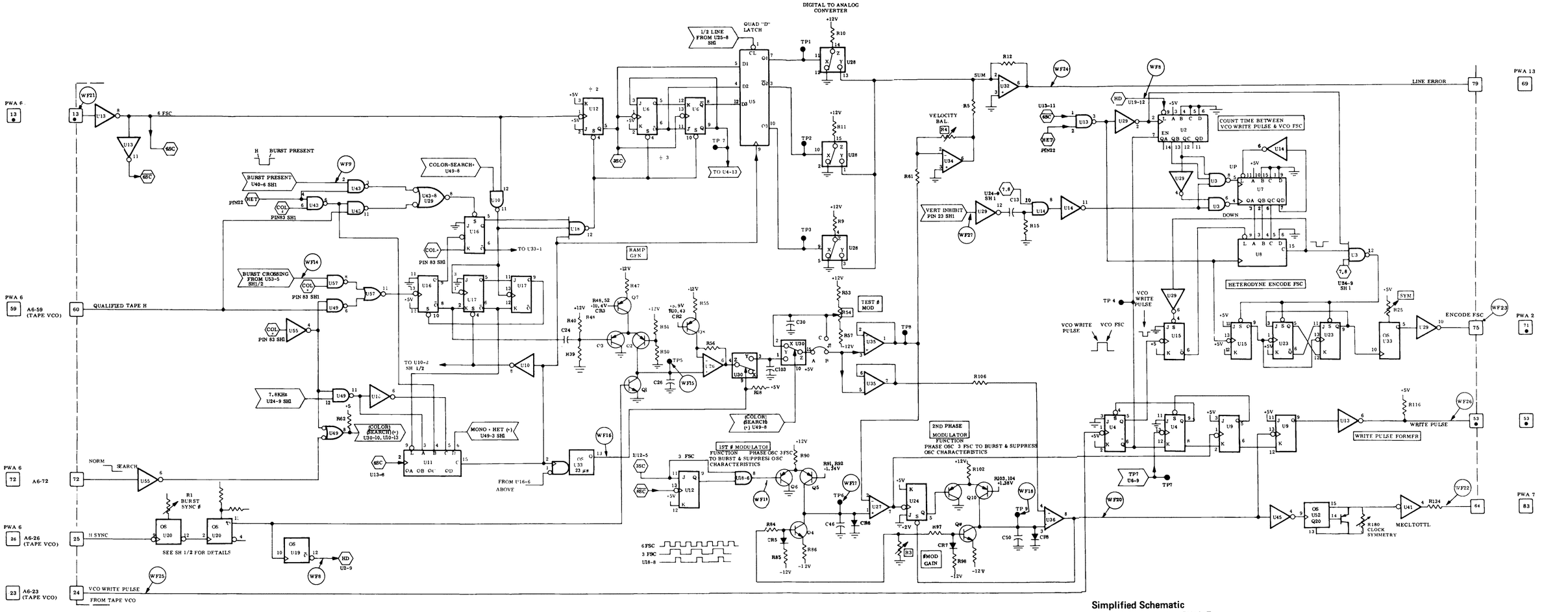
Block Diagram Tape H
Comparator PWA 5
REFERENCE 1



PWA 5 and PWA 6 Signal Relationship, Simplified Block Diagram Tape H Comparator PWA 5 REFERENCE 2



Simplified Schematic
Tape H Comparator PWA 5
REFERENCE 3
(Sheet 1 of 2)



Simplified Schematic
Tape H Comparator PWA 5
REFERENCE 4
(Sheet 2 of 2)

PART II
5-16

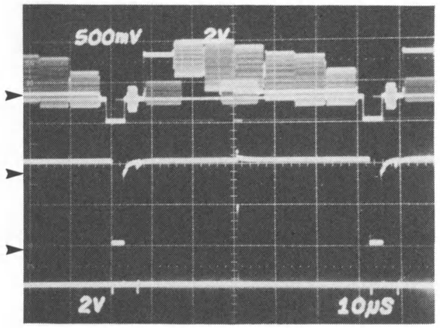
A

THIS TRACE IS VIDEO INPUT PWA 3 TP1

PIN 25
H-SYNC — WF1

PIN 28
1/2 LINE — WF2

TRIG: PIN 25



PIN 69
BURST

U55-8
BURST PRESENT

TRIG: PIN 33

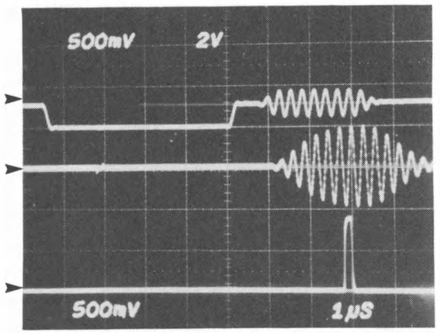
B

THIS TRACE IS VIDEO INPUT PWA 3 TP1

PIN 69
BURST — WF3

TP10
BURST CROSSING SELECTOR — WF4

TRIG: PIN 33



U55-8
BURST PRESENT

U19-12
DELAYED-H

U40-6
BURST PRESENT DETECTOR

TRIG: PIN 33

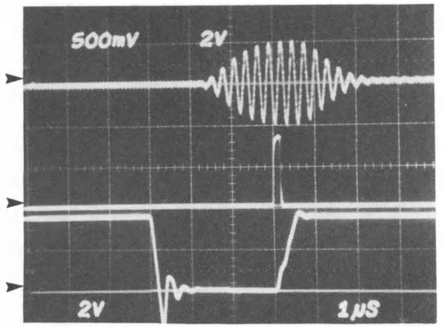
C

PIN 69
BURST — WF3

TP10
BURST CROSSING SELECTOR — WF4

TP11
RAMP — WF5

TRIG: PIN 33



PIN 28
1/2 LINE

U24-9
7.8 kHz

U50-2
2-TO-1 ϕ SWITCH

TRIG: PIN 33

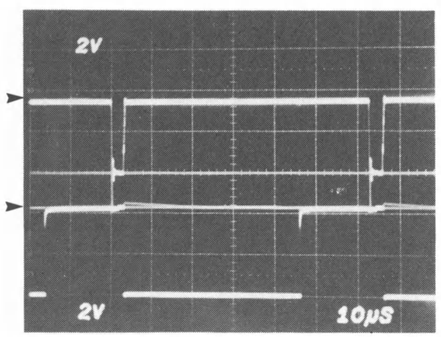
WAVEFORMS H AND I SHOW TWO CONSECUTIVE LINES

D

TP11
RAMP — WF5

U51-9
SAMPLE PULSE — WF6

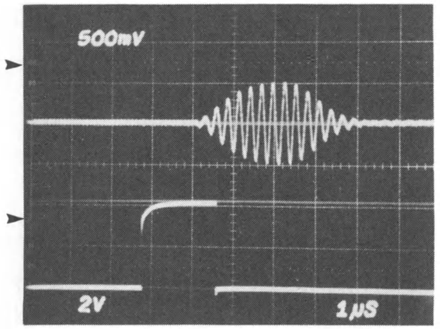
TRIG: PIN 33



E

WF3

WF7



PIN 69
BURST

U55-8
BURST PRESENT

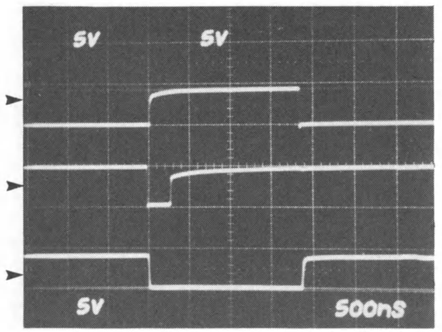
TRIG: PIN 33

F

WF7

WF8

WF9



U55-8
BURST PRESENT

U19-12
DELAYED-H

U40-6
BURST PRESENT DETECTOR

TRIG: PIN 33

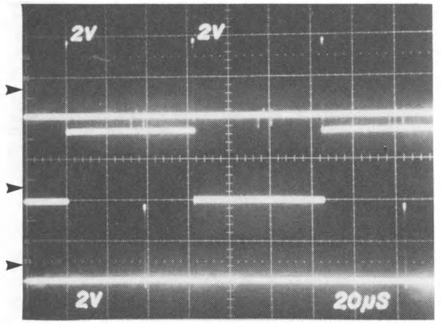
G

PIN 28
1/2 LINE — WF2

U24-9
7.8 kHz — WF10

U50-2
2-TO-1 ϕ SWITCH — WF11

TRIG: PIN 33



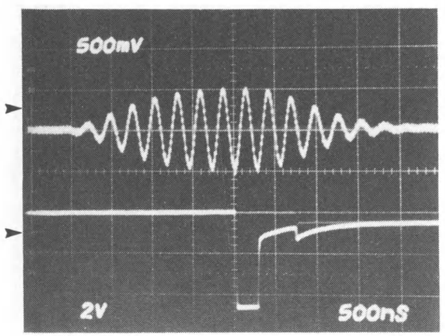
WAVEFORMS H AND I SHOW TWO CONSECUTIVE LINES

H

PIN 69
BURST — WF3

PIN 26
COMPARATOR TIMING — WF12

TRIG: PIN 33

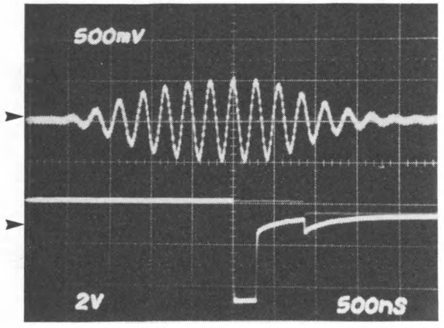


I

PIN 69
BURST — WF3

PIN 26
COMPARATOR TIMING — WF12

TRIG: PIN 33

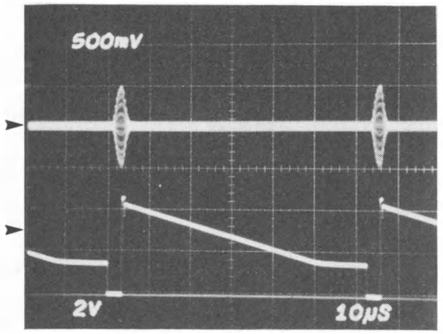


J

PIN 69
BURST — WF3

U53-1
RAMP — WF13

TRIG: PIN 33 (7.8 kHz)
COMPARE WAVEFORM K

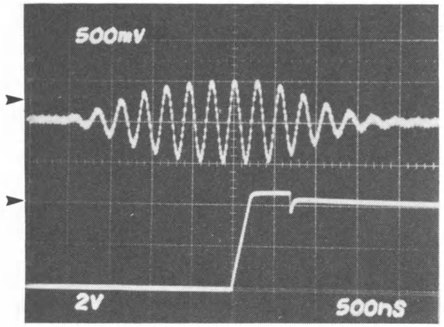


K

PIN 69
BURST — WF3

U53-1
RAMP — WF13

TRIG: PIN 33 (7.8 kHz)
COMPARE WAVEFORM J



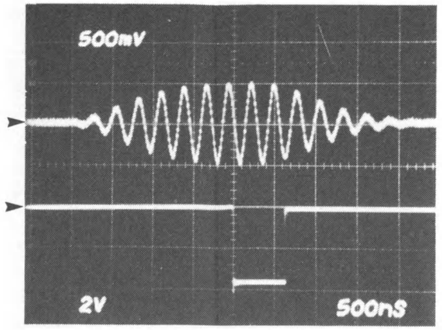
Waveforms
Tape H Comparator PWA 5
REFERENCE 5

L

PIN 69
BURST — **WF3**

U53-5
BURST ϕ CORRECTION
COMPARATOR OUTPUT — **WF14**

TRIG: PIN 33



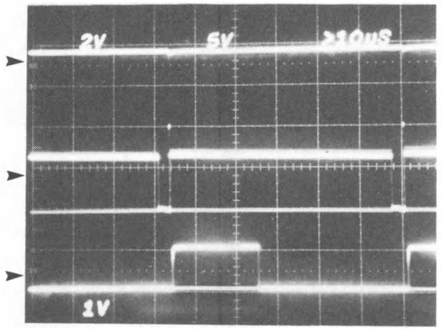
M

U53-5
BURST ϕ CORRECTION
COMPARATOR OUTPUT — **WF14**

TP5
RAMP — **WF15**

U33-13
SAMPLE — **WF16**

TRIG: PIN 33

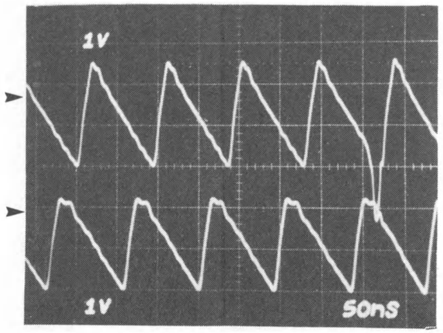


N

TP6
FIRST STAGE
3 Fsc OSCILLATOR — **WF17**

TP9
SECOND STAGE
3 Fsc OSCILLATOR — **WF18**

TRIG: TP8

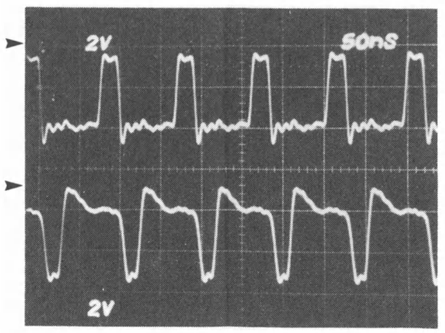


O

U18-8
VCO 3 Fsc AND
6 Fsc — **WF19**

U36-8
SECOND STAGE 3 Fsc
OSCILLATOR OUTPUT — **WF20**

SCOPE EXT TRIG: U18-8

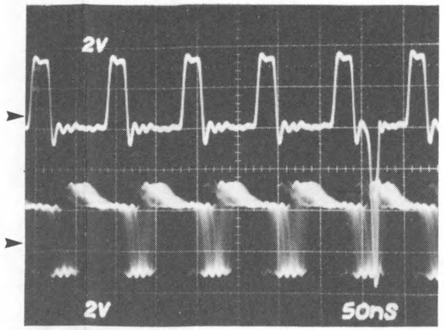


P

U18-8
VCO 3 Fsc AND
6 Fsc — **WF19**

U36-8
SECOND STAGE 3 Fsc
OSCILLATOR — **WF20**

TRIG: U18-8, VTR IN PLAY



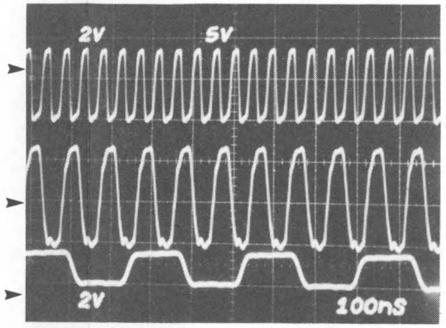
Q

PIN 13
VCO 6 Fsc — **WF21**

PIN 64
TAPE 3 Fsc
(WAVE-SHAPED) — **WF22**

PIN 75
ENCODE Fsc — **WF23**

TRIG: PIN 75, HET/
NORM SW IN HET

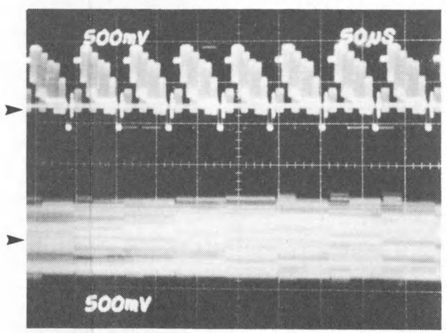


R

PWA 3 TP1
VIDEO INPUT — **WF24**

PIN 79
LINE ERROR

TRIG: PIN 53, VPR IN PLAY



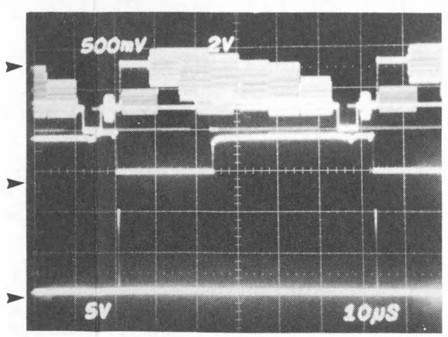
S

PWA 3 TP1
VIDEO INPUT — **WF25**

PIN 24
VCO WRITE PULSE — **WF26**

PIN 53
TAPE-H WRITE PULSE — **WF25**

TRIG: PIN 33

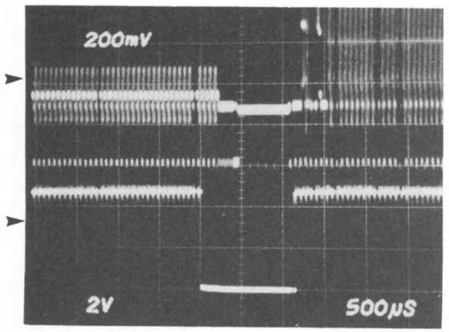


T

**THIS TRACE IS VIDEO
INPUT PWA 3 TP1**

PIN 23
VERTICAL INHIBIT — **WF27**

TRIG: PIN 23,
VPR IN NORM PLAY,
SYNC HEAD OFF

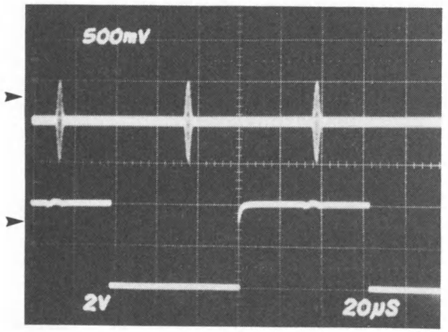


U

PIN 69
BURST — **WF3**

PIN 33
7.8 kHz — **WF28**

TRIG: PIN 33

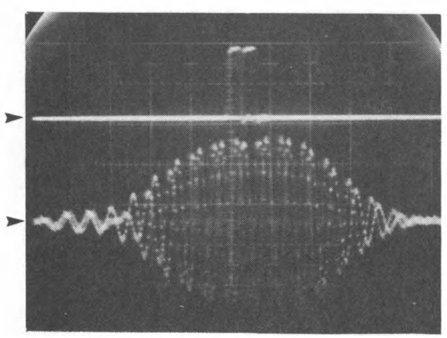


V

TP10
BURST CROSSING
SELECTOR — **WF4**

PIN 69
BURST — **WF29**

TRIG: PIN 25



Waveforms
Tape H Comparator PWA 5
REFERENCE 6

AMPEX 1809474-01

W

U25 PIN 12
R128 CORRECT
ADJUSTMENT

WF30

R128 MISADJUSTED

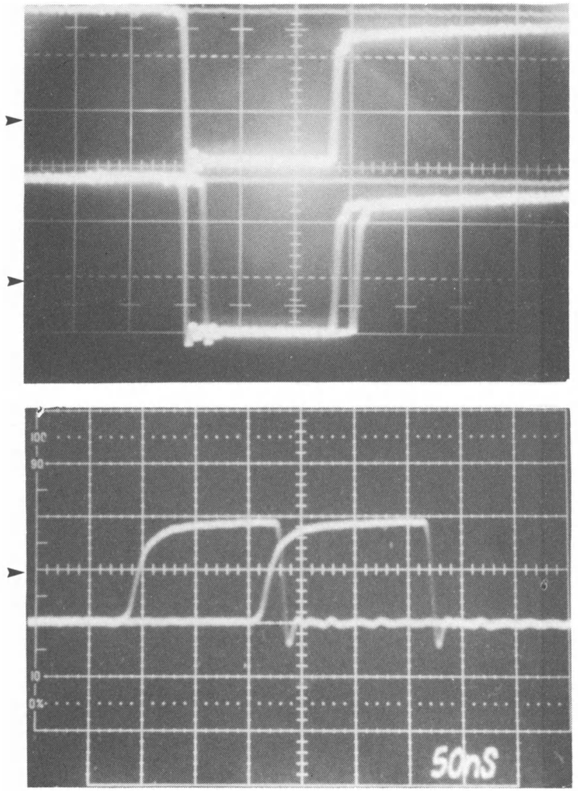
WF30

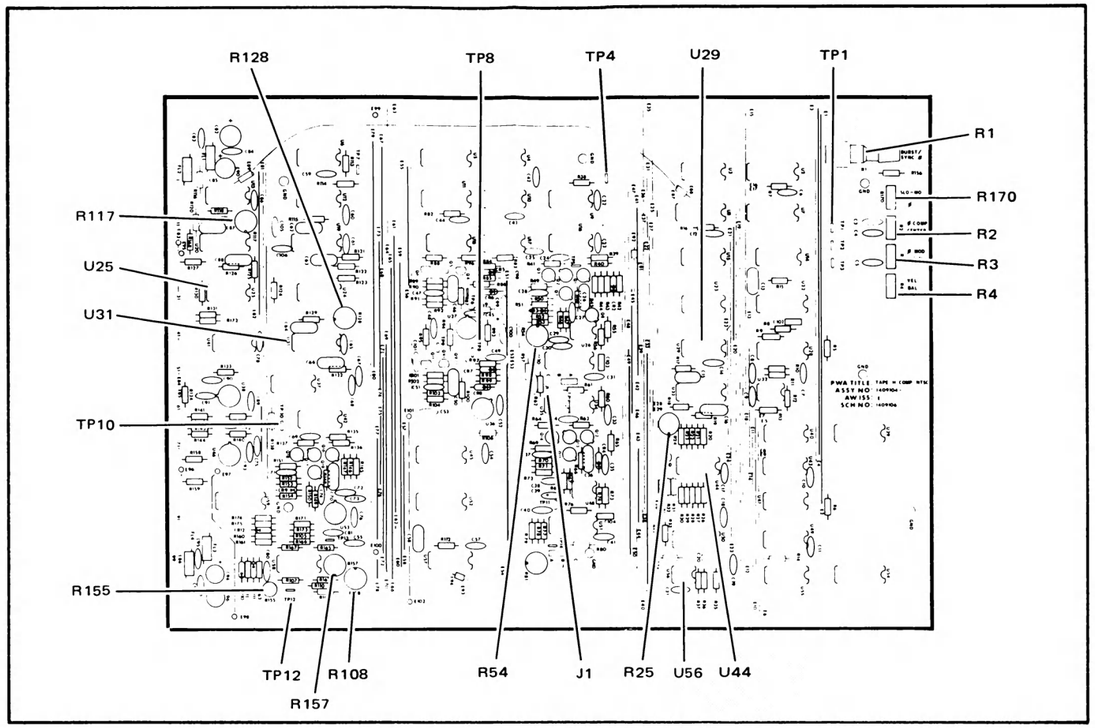
TRIG: U31 PIN 1

X

TP4
RECLOCKED WRITE
PULSE

WF31





PWA 5 Component Locator

PWA 5 Adjustable Components

COMPONENT	FUNCTION	COMPONENT	FUNCTION
R25	Symmetry	R108	DC offset
R54	Test phase modulation	R1	Burst sync phase
R81	Test	R2	Phase comparator center
R117	Burst crossing	R4	Velocity balance
R128	Phase balance	R3	Phase modulator gain
R155	Vector compensation	R180	Clock symmetry
R157	Slow motion dynamic	Notes	
R170	Slow motion static		

PWA 5 Test Points

TEST POINT	FUNCTION
TP1	Vel comp 1/2 line error
TP2	Vel comp line error
TP3	Vel comp 2 line error
TP4	VCO write pulse
TP5	Gated H-rate ramp
TP6	3 X subarrier sawtooth
TP7	Subcarrier pulse
TP8	Line-by-line error
TP9	3 X subcarrier sawtooth
TP10	Burst crossing
TP11	Gated H-rate ramp
TP12	Dynamic error voltage
TP13	Static error voltage
TP14	Error store

PWA 5 Jumpers

JUMPER	POSITION	FUNCTION
J1	A–B B–C	Normal Test – inserts fixed error voltage
J2	A–B B–C	Normal Test – inserts variable DC test error voltage

Waveforms
Component Locator Adjustable Components, Test Points, Jumpers, Tape H Comparator PWA 5
REFERENCE 7

SECTION 6

TAPE VCO

DESCRIPTION AND MAINTENANCE

6-1. INTRODUCTION

Refer to the following documents in the *Parts Lists and Schematics* manual:

ASSEMBLY No. 1409101

SCHEMATIC No. 1409103

Numbered data sheets (REFERENCE 1, 2, 3 . . . *n*) to which PWA descriptions and maintenance procedures refer are located at the end of this section as follows:

Overall Block Diagram – REFERENCE 1

Simplified Schematic – REFERENCE 2, 3, 4

Waveforms – REFERENCE 5, 6, 7

Maintenance Data – REFERENCE 7, 8

TAPE VDC PWA 6
FUNCTION SUMMARY:

- Accepts vertical and horizontal sync from Video Input PWA 3 and playback mechanism and processes it to produce synchronizing signals for use throughout the TBC.

- Contains three oscillators that produce a 6-Fsc signal that is used by the Tape H Comparator PWA to develop the tape 3 Fsc and write pulses. Tape H comparator also develops the encode Fsc signal, used by the Color Processor PWA, from the 6-Fsc signal.

  Normal 6 Fsc oscillator: An LC VCO used in normal operating mode and slo-mo; this oscillator is slaved to selected off-tape burst crossing. Locked to H-sync during monochrome operation.

  Search up oscillator: An RC oscillator from which system write timing is derived during forward shuttling; locked to tape H, produces 6 Fsc.

  Search down oscillator: An RC oscillator from which system write timing is derived during rewind shuttling; locked to tape H, produces 6 Fsc.

6-2. DESCRIPTION

The Tape VCO PWA 6 accepts vertical and horizontal sync from the Video Input PWA 3 and the playback mechanism, and processes it to produce synchronizing signals for use throughout the TBC (see Figures 6-1 and 6-2).

The normal horizontal reference is a selected burst crossing (color burst crossing through the "zero" point of the sine wave). The normal vertical reference is playback vertical which is predicted vertical sync from the playback mechanism. Tape H-sync and tape vertical sync from the Video Input PWA are used in special conditions such as shuttle or monochrome playback.

The Tape VCO PWA has three oscillators. The first is a normal voltage-controlled 6 Fsc LC oscillator, which is phase-locked to the incoming H-rate signal. The basic relationship between H-rate and subcarrier is:

$$H = \frac{2\ Fsc}{455} \qquad H = \frac{2 \times 3\ Fsc}{13 \times 105}$$

$$H = \frac{6\ Fsc}{1365}$$

Fsc = 3.579545 MHz 6 Fsc = 21.47727 MHz
1 cycle = 46.56 nanoseconds

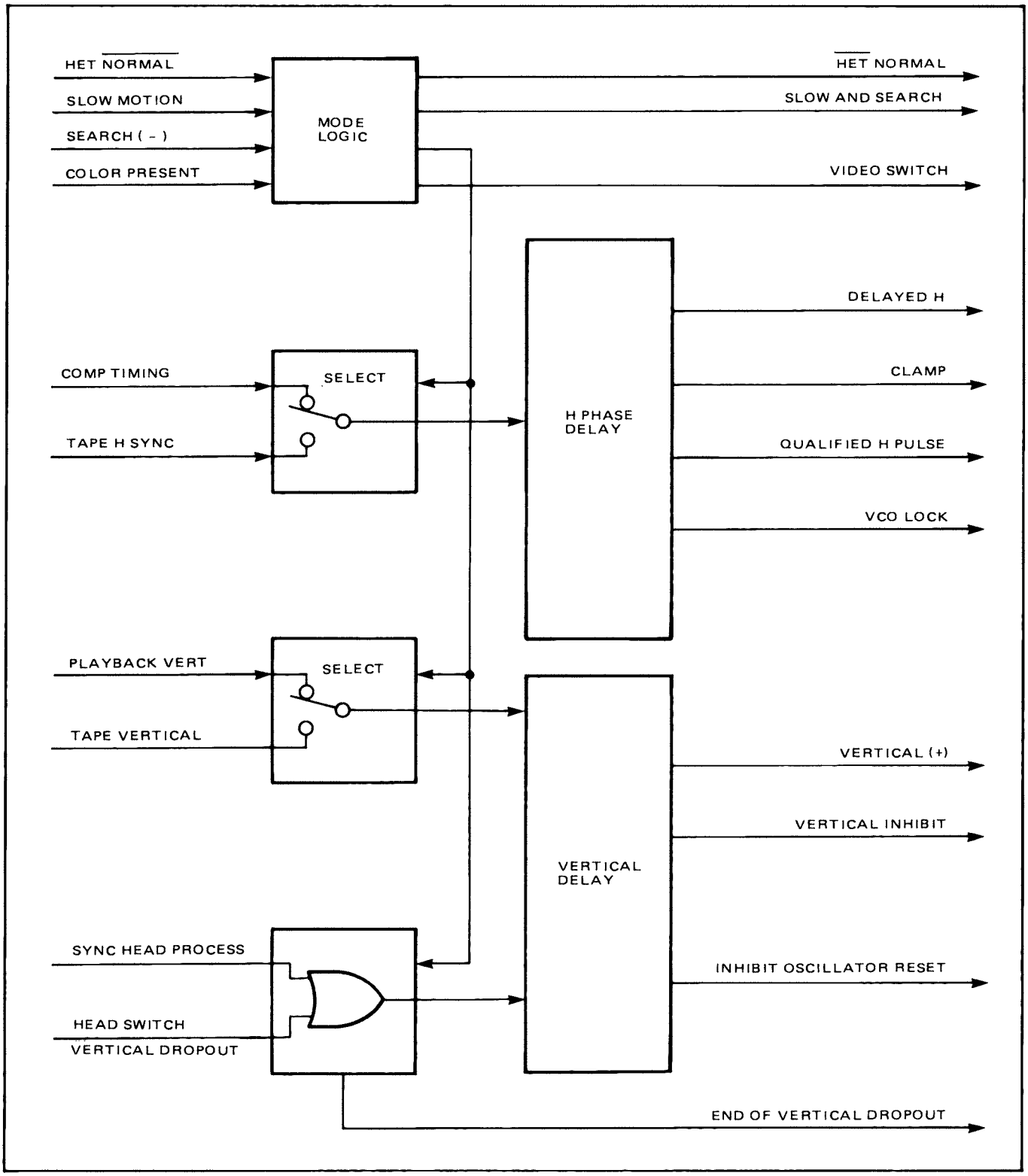


Figure 6-1. Tape VCO PWA 6, Horizontal and Vertical Input Delay Circuits, Simplified Block Diagram

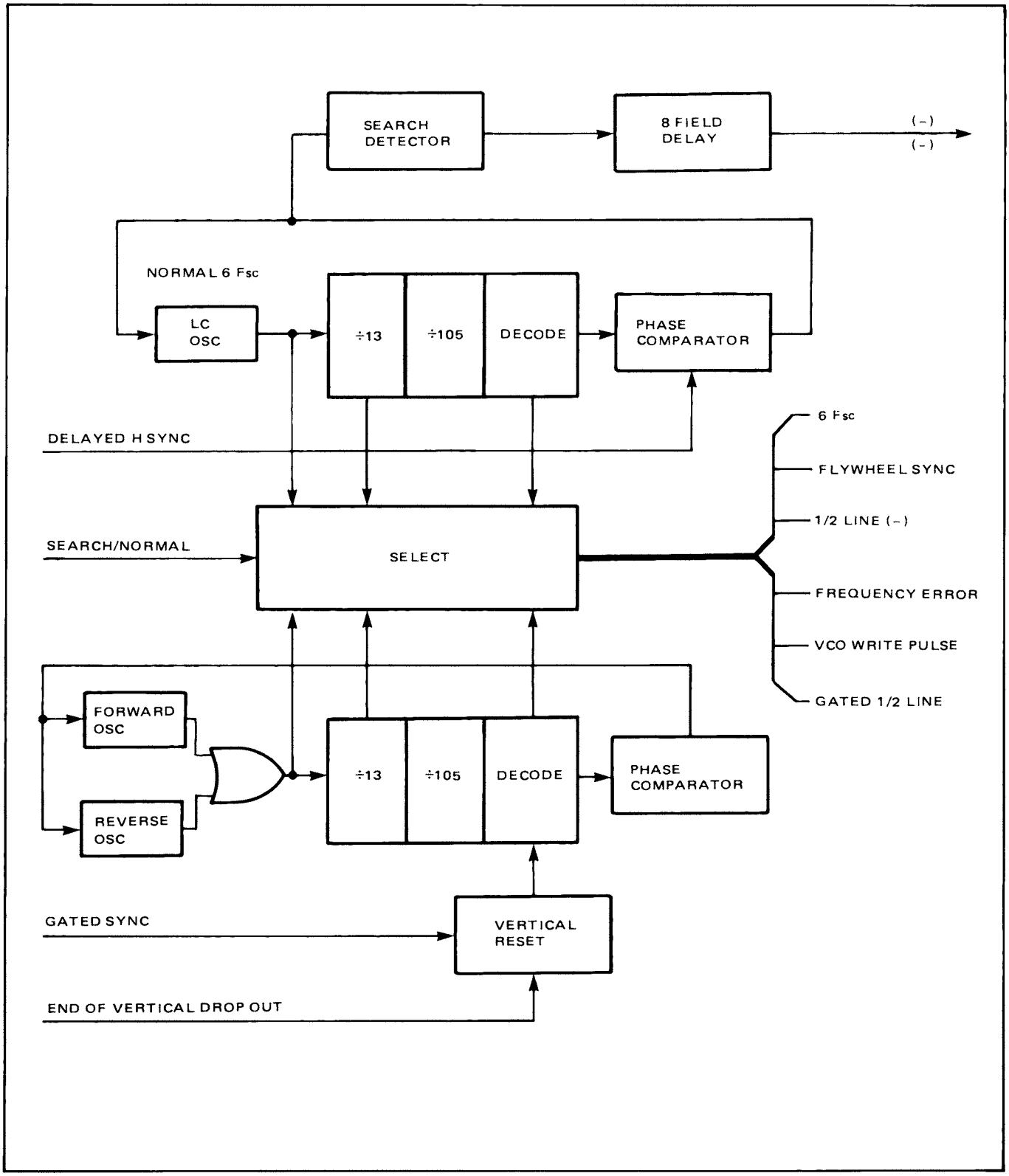


Figure 6-2. Tape VCO PWA 6, Normal and Search Oscillator Circuits, Simplified Block Diagram

The other two oscillators are RC oscillators located in the search oscillator circuitry. The UP/DOWN signal from the VTR selects the oscillator. In fast forward the up oscillator is selected, and in fast reverse the down oscillator is selected. The normal 6-Fsc oscillator operates until an error threshold is reached. This error threshold enables the search oscillator and switches control of the Tape VCO output synchronizing signals from normal oscillator circuits to search oscillator circuits. The output of the normal 6-Fsc oscillator is applied to a divide-by-13 counter. The 8-bit count (1.65-MHz rate) clocks the divide-by-105 counter. The final count of 1365 resets the divide-by-105 counter and loads an initial count of 25. The divide-by-13 counter is reset by its carry output and loads an initial count of 3. The count of 1365 is one horizontal line in time and is therefore a prediction of the time of arrival of the delayed H-rate pulse. The digital phase comparator generates an error voltage proportional to the phase difference of these signals and thereby forms a closed loop which locks 6-Fsc oscillator in phase with the incoming H-rate signal. The synchronizing signal for all except the format gap during the vertical interval is the color burst crossing. The 6-Fsc oscillator is therefore in phase with the tape color burst. All of the timing components of the television signal are derived from the subcarrier frequency. The frame rate is H/525, and the field rate is 2H/525. In addition, in the TBC the Tape H Comparator PWA 5 drives a 3-Fsc signal from the Tape VCO 6 Fsc which is used by the A/D Converter PWA 4 to sample the video at 3 Fsc rate (10.7 MHz) prior to placing the digitized information in memory.

Several forms of timing error are introduced in the process of video tape recording; one is impact-generated by the head entering or leaving the tape and other mechanical irregularities inherent in the recording and playback process; another is program material from recordings that may not be properly time-base corrected. In slow motion or freeze the field is reproduced with an incorrect tape speed. In freeze the tape is stationary and there is a 1% error in tip-to-tape velocity; therefore a horizontal line is lengthened by 1%, subcarrier (burst) frequency is changed by 1%, and the field is reduced by 1% (2-1/2 lines). Video written into memory in digital form must be synchronized to the playback subcarrier although, because of time distortion, that subcarrier frequency is not precisely 3.579545 MHz. The only measure of the subcarrier and its distortion by the record/reproduction process is the 9 to 10 cycles of burst on the back porch of the horizontal sync. In lines 1 through 9 color burst is not available; in addition, the helical recorder format gap occurs in lines 3 through 14. The horizontal synchronizing signal is switched from burst crossing to Tape H Sync in lines 2 through 9, allowing the Tape VCO PWA to maintain the integrity of its synchronizing outputs during the vertical interval. (See Waveforms U and V.)

6-3. Decoding — Normal 6 Fsc Oscillator

In the normal 6-Fsc circuit, various outputs of the counter are decoded to provide synchronizing signals within the TBC-2. Because the Tape VCO is slaved to burst crossing, the "predicated" delayed H-pulse (1365) is generated approximately 7.6 microseconds after the leading edge of horizontal sync (see Waveform H and Figure 6-3). A decoded count of 507 provides the 1/2-line pulse. The decoded count of 1201 provides flywheel sync which, if all is well, will be coincident with the leading edge of horizontal sync. The decode of 1352 triggers the "window" of the tape-H quality circuit (see Waveforms I, M). The 1.65-MHz signal (8 bit of the divide-by-13 counter) is applied to a frequency discriminator to produce a frequency error signal to the Tape H Comparator PWA. It is also used, when no external input is available, to determine tape direction in fast forward or reverse. The discriminator output is nominal 6.5 volts in normal tape speed with a 200 mV change per 1% change in oscillator frequency.

A decoded count of 3 from the divide-by-13 counter is gated by 7.8 kHz from the Tape H Comparator. At the time of the count of 1365 the 7.8 kHz will be high for one line and low for the next. If 7.8 kHz is high, the count of three will be AND'ed with the 1365 pulse. The start of the VCO write pulse will be 140 ns late (1/2 cycle of Fsc). If 7.8 kHz is low, the start of the VCO write pulse will be initiated by the leading edge of the 1365 pulse. The half cycle shift of data written

into memory will, when read out of memory, provide exact registration of chroma interlace.

6-4. Search Oscillator

As stated previously, the search oscillator circuitry has two RC oscillators. If the TBC is used with a slow-motion playback mechanism an $\overline{UP}$/DOWN signal will select the appropriate oscillator. If it is used with a heterodyne mechanism, the frequency error signal will automatically select the correct oscillator. The feedback loop and decoding is similar to that used in the normal 6-Fsc circuit, but with some significant differences. The counters are the same type – divide-by-13, preset to 3, and divide-by-105, preset to 25. A decode count of 507 provides the search 1/2-line pulse. The decoded count of 1201 provides search flywheel sync, coincident with the leading edge of the horizontal sync. At the count of 507 the K-input of a JK flip-flop is set high. At the count of 1144, $\overline{Q}$ is clocked high, $\overline{Q}$ is AND'ed with the count of 1201 to produce flywheel sync. A decoded count of 1355 sets the VCO write pulse flip-flop; the following 1/2-line pulse resets it.

At the final count of 1365, the divide-by-105 counter is reset and loaded with a count of 25. Since the clock for the divide-by-105 counter is the eight-count of the divide-by-13 counter, after 5 more counts the carry output resets the divide-by-13 counter and leads it with a count of 3. The eight-count also provides the search 1.65-MHz signal. The count of 1365 also presets the JK flip-flop which had been clocked by the 1144 count.

A flip-flop is preset by the end of vertical dropout signal and clocked by the next gated sync pulse. This enables a divide-by-14 counter. The carry

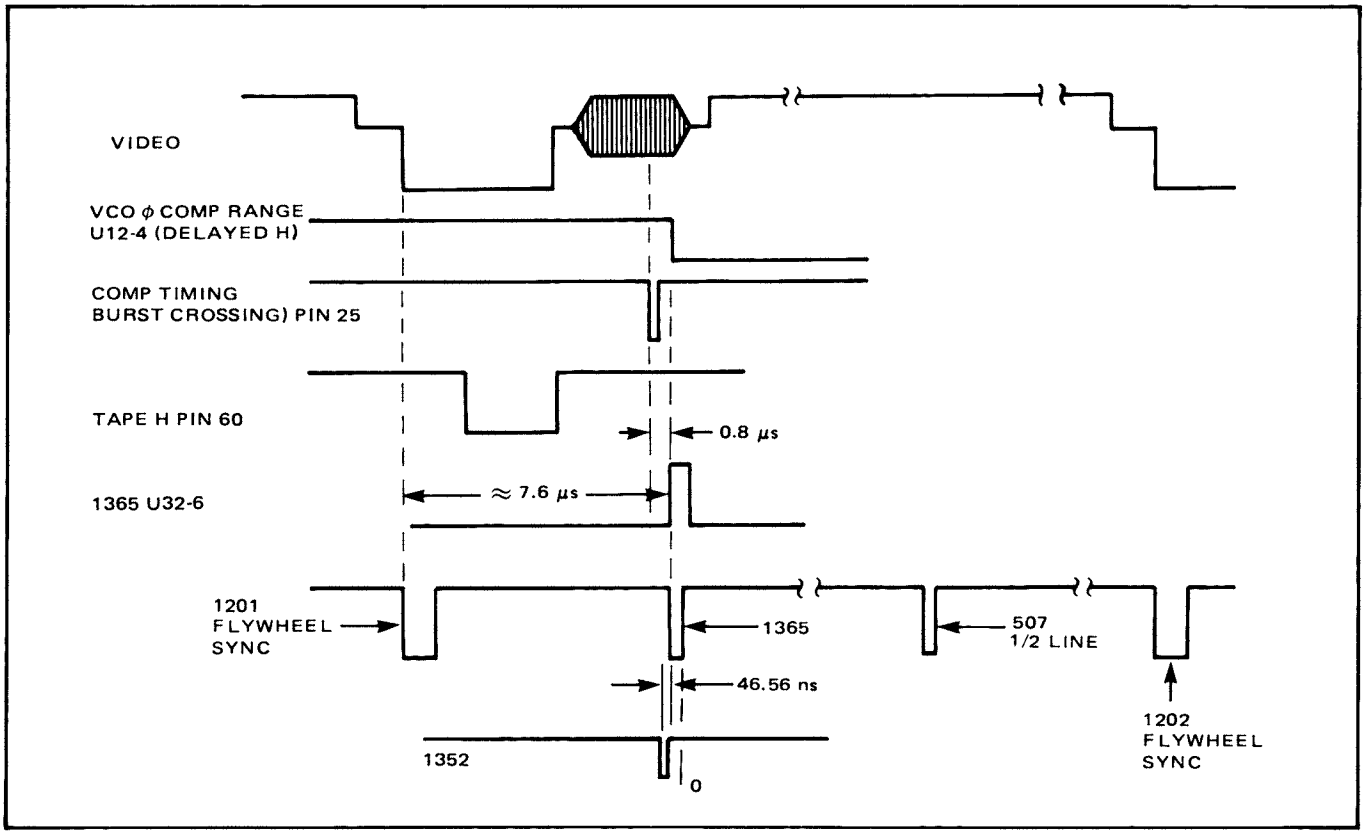


Figure 6-3. Counter Decode Timing Relationship

output, 8.5 microseconds later, resets the divide-by-105 counter. Thus, only in the vertical interval in each field of a color picture is the decode circuitry phase-locked to horizontal sync.

The count of 1144, which is coincident with the start of the horizontal blanking period, starts a ramp generator (see Waveform P). The ramp terminates near the trailing edge of horizontal sync. The ramp generator is reset at 1/2-line time. The gated sync signal operates a sample-and-hold circuit during the ramp period. In fast forward operation of the tape transport the gated sync will "arrive early" and will sample a higher positive value of the ramp. In fast reverse the sample will occur "late" and will therefore sample a lower positive value. In fast forward, the $\overline{\text{UP}}$/DOWN signal will switch in 1.2 volts as constant to the sample storage capacitor. In fast reverse a constant of 0.47 volt from the voltage divider is switched in. Thus, it can be seen that as the tape H rate increases a higher positive signal will increase the frequency of the up oscillator — and as the tape H-rate decreases, a lower positive value will lower the frequency of the down oscillator.

6-5. Horizontal Sync — Video Field

During video field time (line 20 to 262), if in normal operation with color present, the burst crossing signal (pin 25) from the Tape H Comparator is selected to drive circuits associated with H-rate timing. Through a series of delay one-shots, the signal is phased to create a flywheel sync pulse at video H-sync time. The delayed H-pulse is applied to one input of a digital phase comparator. A counter, driven by the 6-Fsc oscillator, generates the normal flywheel sync pulse (1201 counts of the 6 Fsc oscillator) and a measured interval later a counter reset pulse (1365 counts) which is also the other input to the digital phase comparator. The output of the comparator is integrated and applied as an analog dc voltage to a varactor in the 6-Fsc oscillator circuit. Thus, an accurate phase relationship between the burst crossing signal and the 6-Fsc oscillator is maintained.

The integrated output of the digital phase comparator is also sent to a "window" voltage comparator. The normal output of the integrator is 4 volts; the window limits are +4.5V and +2.5V. If the integrator output falls outside these limits, an eight-field delay counter is enabled. The carry output triggers a 1.2-second one-shot which provides the search positive (+) and negative (–) signals. The search signal is activated in shuttle operation of the playback mechanism when the incoming H-rate is too high (fast shuttle forward) or too low (fast shuttle reverse).

When in search mode the following conditions are established:

- UP/DOWN gates of the search oscillator are enabled.
- Field rate input to the 256 vertical delay counter is switched from playback vertical to tape vertical.
- Search 1/2-line instead of normal 1/2-line to 256 vertical delay, normal VCO write pulse flip-flop, search VCO write flip-flop, and flywheel sync flip-flop.
- Search 1.65 MHz instead of normal to the frequency discriminator.
- Search flywheel sync instead of normal to the flywheel sync one-shot.
- Search 6 Fsc instead of normal to pin 13.
- Search VCO write pulse instead of normal to pin 23.
- VCO lock to pin 71 is inhibited.
- Search (–) is gated to pin 72.

The H-sync signal, whether from burst crossing (pin 25) or tape H-sync (pin 60), is delayed approximately 0.6 microseconds by the H-reset and qualify delay one-shot. $\overline{\text{Q}}$ drives the digital phase comparator; Q provides the tape pulse to the qualify H-pulse circuit. The count of 1352 of the 6 Fsc oscillator (46.65 ns prior to the next predicted delay H-pulse) provides a 586-ns gate to "qualify" a 104-ns pulse triggered by the H-reset and qualify delay one-shot. If coincidence occurs, a flip-flop will be reset by the qualified H-pulse and

clocked "set" by the VCO comparator range one-shot approximately 31 microseconds later. Thus, the VCO comparator is enabled 0.6 microseconds before the predicted time of the delayed H-pulse and is inhibited 32 microseconds later. This operation is referred to as line-by-line qualification. If coincidence does not occur (not qualified), the phase comparator is not enabled for the succeeding line. The signal used to enable/inhibit the digital phase comparator is gated out to pin 56 as the clamp pulse to the color processor. The qualified H-pulse is also used to trigger a 1.5-ms one-shot which is gated out to pin 71 as VCO lock to the video input. If the H-pulse is not qualified the VCO lock one-shot is inhibited.

6-6. Horizontal Sync — Vertical Blanking Interval

The vertical inhibit signal is reclocked with 1/2 line (+), and with the reset qualify signal generated in the vertical delay circuits is used during the vertical blanking interval to inhibit the digital phase comparator (see Waveform K). Thus, during the period when the VTR's playback head enters and leaves the tape, the oscillator will not be skewed by absent or distorted timing signals. In addition, a switch signal beginning with line 2 (start of head switch vertical dropout) and ending at the end of line 9 (trailing edge of playback vertical) replaces burst crossing with tape H-sync to drive the horizontal sync circuits. Vertical inhibit is also gated out to the tape H comparator (pin 24) and to the video input and color processor (pin 55).

6-7. Heterodyne Operation

Sync head process (pin 73) (VPR) and head switch vertical dropout (pin 69) (VPR) are inhibited, therefore end of vertical delay — the trailing edge — clocks one reset qualify pulse.

6-8. Normal Operation — Vertical Delay

If not in search, heterodyne, or slow-motion mode, playback vertical (pin 33) or tape vertical (pin 57) may trigger the 256-count vertical delay circuit. If in search mode, tape vertical only is used. If in slow motion (and not search), playback vertical only is used.

At leading edge of playback vertical (or tape vertical) if in normal mode, the 256-count vertical delay is loaded to zero and clocked by 1/2-line (+) pulses. At the 256 count the carry pulse triggers a one-shot which forms the vertical inhibit signals (pin 24 and 55). These outputs are used to inhibit various circuits during the period when one playback head is leaving the tape and another is entering it.

6-9. Normal Operation — Reset Qualify

If the sync head is in use, sync head process (pin 73) is low, enabling head switch vertical dropout (leading and trailing edges) and playback vertical (trailing edge) to produce three reset qualify pulses during the vertical blanking interval (see Waveform C). If the sync head is not in use, sync head process goes high, inhibiting sync-head process gating so that only the trailing edge of the head switch vertical dropout produces a reset qualify pulse. The reset qualify pulse is started as previously described. After a 2H delay it may be ended if a qualified H-pulse is received from the tape H pulse qualify circuits. If no qualified H-pulse is received, the reset qualify pulse will continue for a total of up to 15H, at which time it will be arbitrarily terminated.

The reset qualify signal provides an inhibit of the error control of the normal 6-Fsc oscillator and prevents disqualification of the VCO lock signal during the vertical blanking interval. In addition, it provides insurance against a loss of flywheel sync. The flywheel sync generator is enabled at 1/2-line time (507 count). If for any reason the decoded 1201 count does not trip the flywheel sync one-shot, and thereby latch it shut until the next 1/2-line time, 4 microseconds later a tape H pulse will be enabled into the OR gate by reset qualify. If that pulse fails, a comp timing (burst crossing) pulse (see Waveform E) reclocked by 6 Fsc and the eight-count of the divide-by-13 counter will be gated into the OR gate. If that one fails, a last attempt will be made by the 1365 count pulse. The reason for providing the redundant circuits to develop a flywheel sync is that every line of the field must be written into memory in its exact sequence, otherwise the write-read-sequence of memory would be impaired.

6-10. TAPE VCO MAINTENANCE

See REFERENCE 5, 6, 7, 8 in this section for the component locator diagram, jumper/test-point/ adjustable component summaries, and the waveforms called out in these procedures.

Before undertaking any adjustments to the Tape VCO review the *System Alignment Guide* (Table 3-2) and the *Tape/Reference Test Loop* discussion (paragraph 3-5) in the *System Maintenance* section (Part I) for a general understanding of the scope of these field adjustments.

Consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the Tape VCO and interactive functions between it and other PWA's before making adjustments. Pay particular attention to the Tape H Comparator and Video Input PWA's. Adjustment to or replacement of the Tape VCO PWA may require complementary adjustment to the Tape H Comparator PWA.

6-11. VCO and Frequency Error Discriminator Alignment

1. Use tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN.

2. Normal mode VCO alignment:

   a. With power off, remove Tape VCO PWA 6. Connect a digital voltmeter to TP1 and ground. With DVM still connected to TP1, insert PWA back into frame.

   b. Switch power on and allow a 2-minute warmup of TBC.

   c. Switch MODE to NORMAL.

   d. Verify a +4 (± 0.1) volt dc level at TP1. Adjust L1 (normal 6 Fsc oscillator), if necessary, using nonmetallic tuning tool AF-12-H.

3. Frequency error discriminator calibrations:

   a. With power off, remove PWA and connect a miniature clip lead or solder a wire to connector end of R120 (1K 5% 1/8 watt resistor – see component locator). This end of resistor is electrically at edge connector pins 79, 80. Connect wire to a digital voltmeter and insert PWA back into frame. Allow a 2-minute warmup of the TBC and then read dc level at connector end of R120. It should be 6.5 volts ± 0.05 volts.

   b. Adjust L2 (frequency error), if necessary, using nonmetallic tuning tool AF-12-H. It may be necessary to alternately adjust and reinsert PWA more than once to obtain desired reading.

   NOTE

   If adjustments are to be made to Tape H PWA, leave clip lead attached for later test.

4. Tape H reset and qualify delay adjustment:

   a. Connect oscilloscope –

      Channel 1: TP1 (VCO dc error)

      Trigger: PWA pin 57 (tape vertical)

   b. Adjust R45 (tape H reset and qualify delay) through its range and note the presence of vertical rate pulses. Set R45 so that the vertical pulses are at minimum amplitude (nominally 50 mV).

   c. Connect oscilloscope –

      Channel 1: TP5 (gated tape H reset)

      Trigger: PWA pin 25 (Tape H comparator timing)

   d. Adjust R50 (VCO phase comparator range) for a 50% duty cycle. Waveform 4(B) shows a typical adjustment. The 50% duty cycle sets up a symmetry for

the error signal at TP1 for clipping on both positive and negative peaks.

5. Go to PWA-level Tape H Comparator adjustment section and verify normal operation of burst/sync phasing (paragraph 5-7).

6-12. Vertical Delay

Vertical delay control establishes vertical inhibit timing of format dropout and is used for heterodyne or other VTR's without a sync head and may be adjusted any time, but should be done before line error velocity compensation adjustment.

1. Use tape/reference test loop setup with a 75% color-bar signal to TAPE VIDEO IN.

2. Connect oscilloscope –

   Channel 1: TP10 (vertical inhibit)

   Channel 2: PWA 3 TP1

   Trigger: TP10

3. Adjust R88 so that trailing edge of inhibit ends after rf recovery and one line prior to active video. Waveform 25(Y) shows a typical setting at line 16 for a VPR without a sync head. For VPR's with a sync head inhibit is coincident with start of line 10.

6-13. Shuttle Mode Verification with the VPR

This verification requires normal VPR/TBC configuration with both units fully operational and properly phased to system reference (RS170A sync/burst phase or facility standard reference).

1. Make a 10-minute color-bar recording.

2. With power off extend tape VCO.

3. Connect an oscilloscope to TP4 (search sample pulse); trigger on internal. Pulse is shown in WF24(0).

4. Set VPR TAPE/EE switch to TAPE.

   NOTE

   If VPR has a sync head perform steps 5-9 below for sync head both on and off.

5. Shuttle recording (rewind) and verify a stable monochrome picture with normal, random narrow black streaks across it.

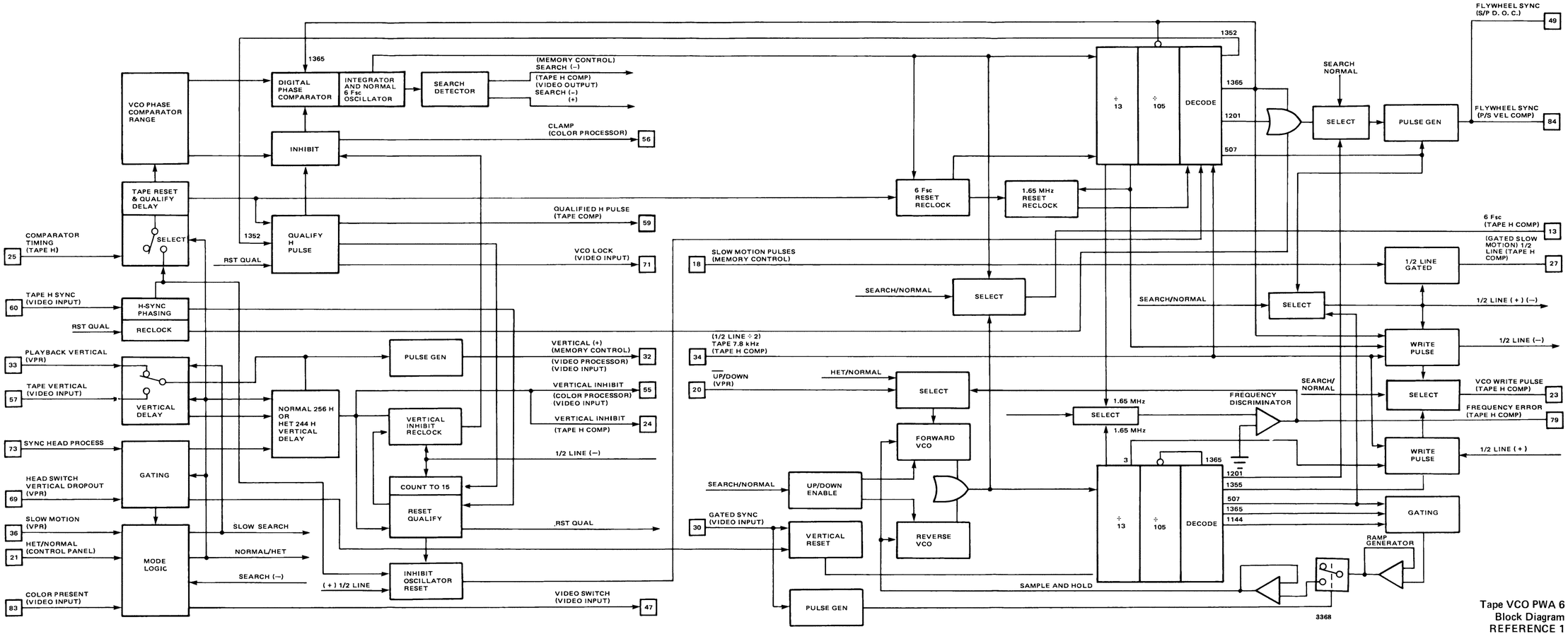
6. Verify that SEARCH indicator (PWA Edge, red LED) is on.

7. Verify that a stable monochrome picture still exists when period of search sample pulse is 93 microseconds.

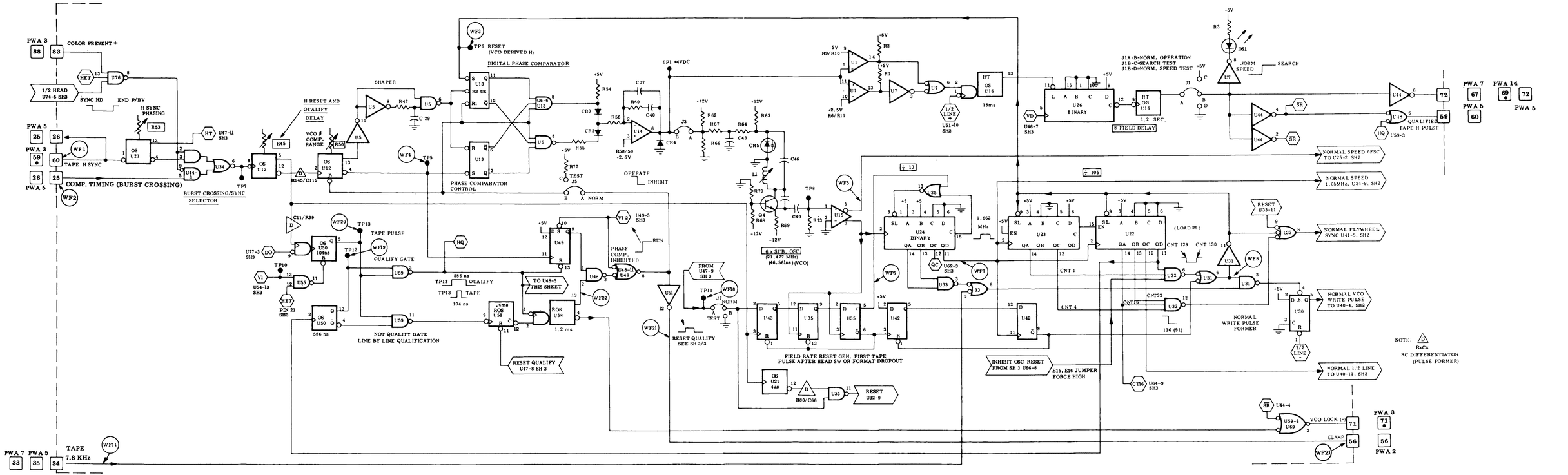
8. Shuttle recording forward. Verify stable monochrome picture with black streaks and that SEARCH indicator is on.

9. Verify stable picture for a search sample pulse period of 47 microseconds.

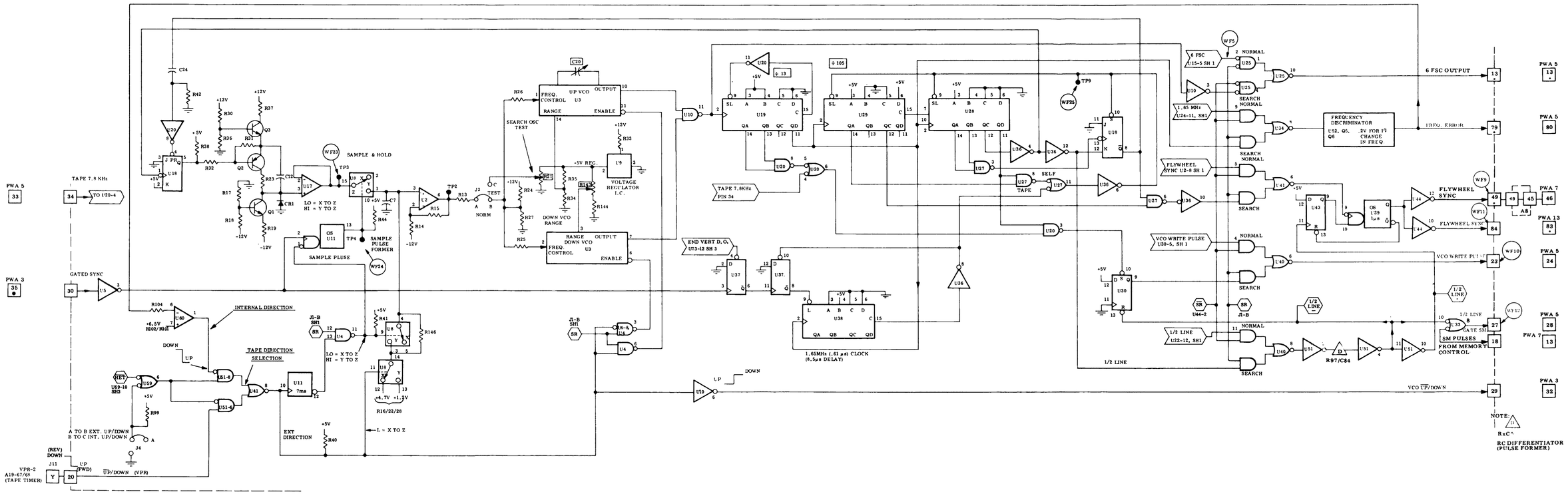
10. With power off return PWA to cage.



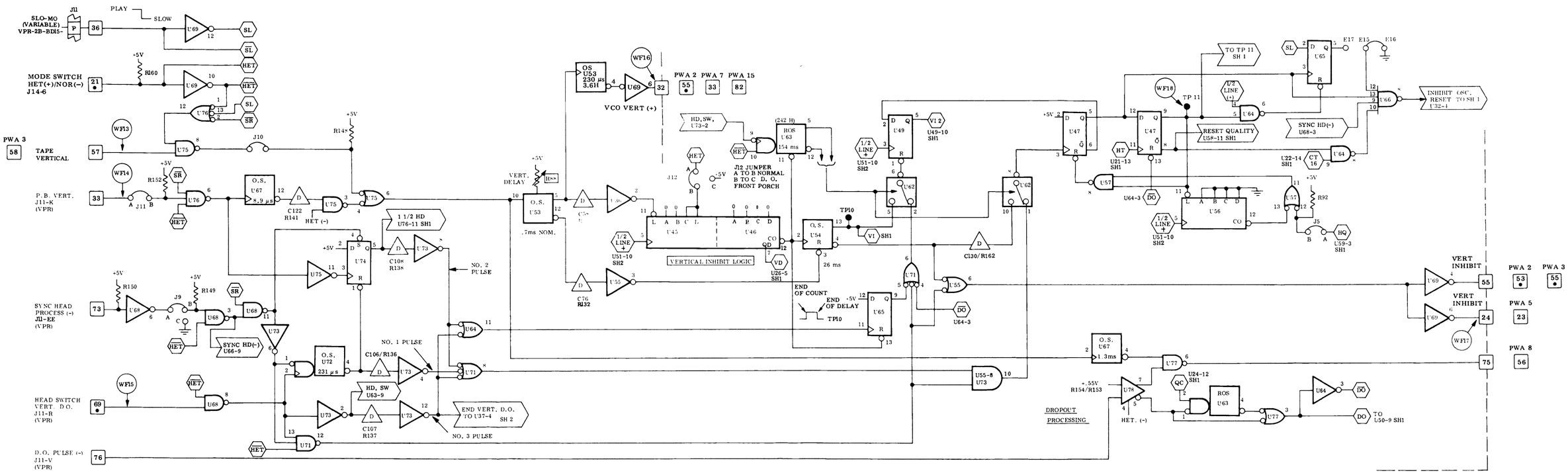
Tape VCO PWA 6
Block Diagram
REFERENCE 1



Normal Speed VCO and
Search Counters Simplified Schematic
Tape VCO PWA 6
REFERENCE 2



Tape VCO Search Oscillators and Horizontal Counters Simplified Schematic
Tape VCO PWA 6
REFERENCE 3



Vertical and Dropout Logic
Simplified Schematic
Tape VCO PWA 6
REFERENCE 4

AMPEX 1809474-01

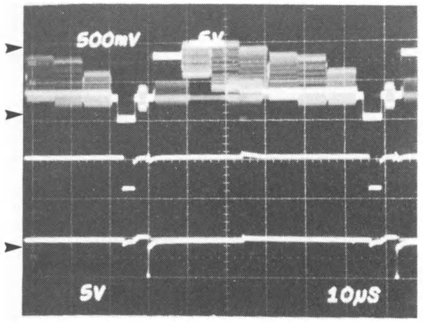
A

THIS TRACE IS VIDEO INPUT PWA 3 TP1

PIN 60
TAPE H SYNC — **WF1**

PIN 25 — **WF2**

TRIG: PIN 25



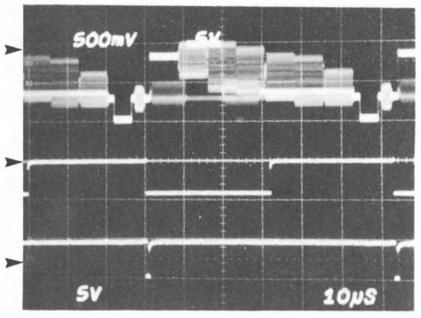
B

THIS TRACE IS VIDEO INPUT PWA 3 TP1

TP6
VCO DERIVED H RESET — **WF3**

TP5
GATED TAPE H RESET — **WF4**

TRIG: PIN 25

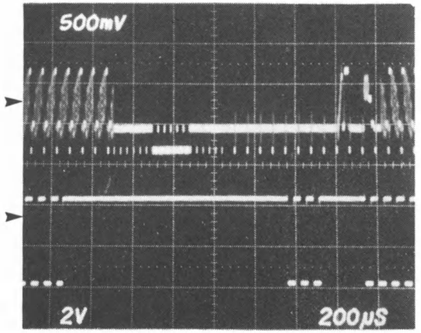


C

THIS TRACE IS VIDEO INPUT PWA 3 TP1 — **WF1**

TP5
GATED TAPE H RESET — **WF4**

TRIG: TP11, VPR IN NORMAL/PLAY, SYNC HEAD ON

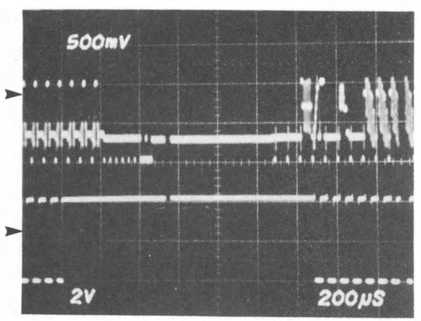


D

THIS TRACE IS VIDEO INPUT PWA 3 TP1 — **WF1**

TP5
GATED TAPE H RESET — **WF4**

TRIG: TP11

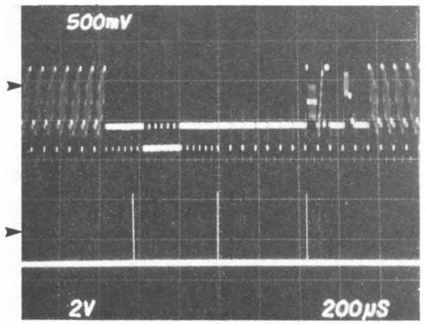


E

THIS TRACE IS VIDEO INPUT PWA 3 TP1

U35-5
RECLOCKED, DELAYED COMPARATOR TIMING — **WF6**

TRIG: TP11, VPR IN NORM/PLAY, SYNC HEAD ON PHOTO MODIFIED TO SHOW NARROW PULSES (WF6)

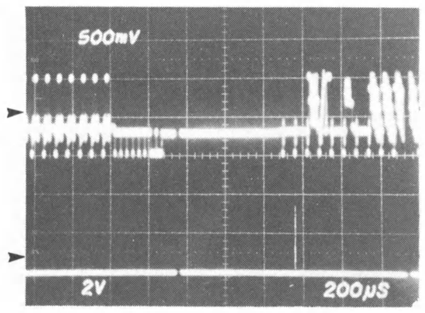


F

THIS TRACE IS VIDEO INPUT PWA 3 TP1

U35-5
RECLOCKED DELAYED COMPARATOR TIMING — **WF6**

TRIG: TP11, VPR IN NORM/PLAY, SYNC HEAD OFF PHOTO MODIFIED AS ABOVE

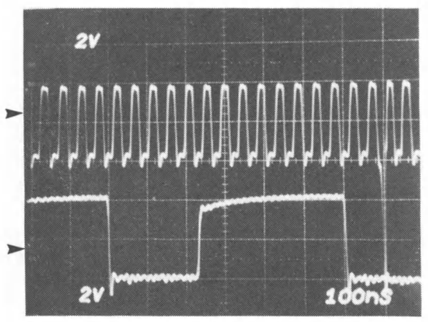


G

U15-5
Fsc OSCILLATOR OUTPUT — **WF5**

U24-11
1.65-MHz NORMAL ÷ 13 COUNTER — **WF7**

TRIG: U24-11

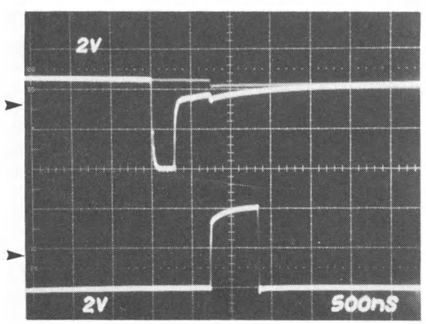


H

PIN 25
COMPARATOR TIMING (BURST CROSSING) — **WF2**

U31-6
NORMAL COUNTER DECODE — **WF8**

TRIG: U31-6



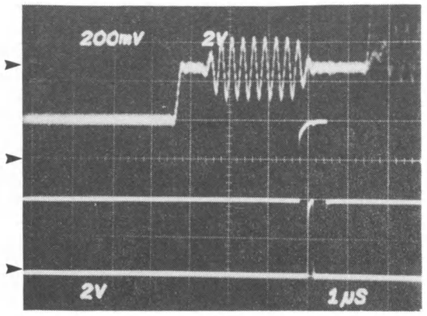
I

THIS TRACE IS VIDEO INPUT PWA 3 TP1

TP12
QUALIFY PULSE — **WF19**

TP13
TAPE PULSE — **WF20**

TRIG: TP13, VPR IN NORMAL PLAY



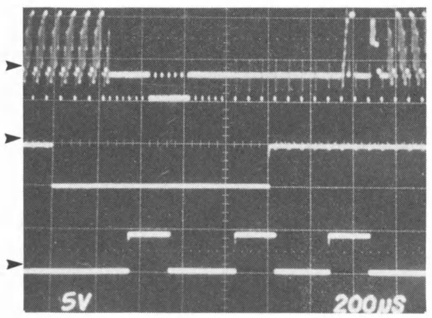
J

THIS TRACE IS VIDEO INPUT TP1

PIN 24
VERTICAL INHIBIT (END OF V DELAY) — **WF17**

TP11
RESET QUALIFY — **WF18**

TRIG: TP11, VPR IN NORMAL PLAY, SYNC HEAD ON



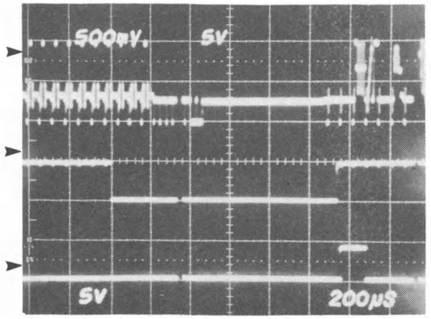
K

THIS TRACE IS VIDEO INPUT TP1

PIN 24
VERTICAL INHIBIT — **WF17**

TP11
RESET QUALIFY — **WF18**

TRIG: TP11
VPR IN NORMAL PLAY SYNC HEAD OFF



Waveforms,
Tape VCO PWA 6
REFERENCE 5

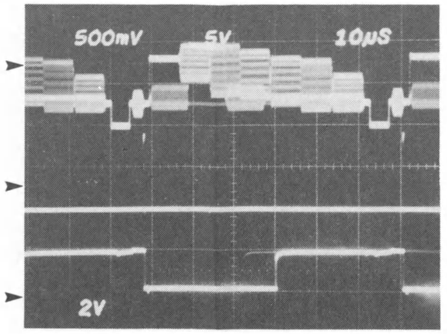
M

THIS TRACE IS VIDEO INPUT PWA 3 TP1

TP13
TAPE PULSE — WF20

PIN 56
CLAMP — WF21

TRIG: TP13



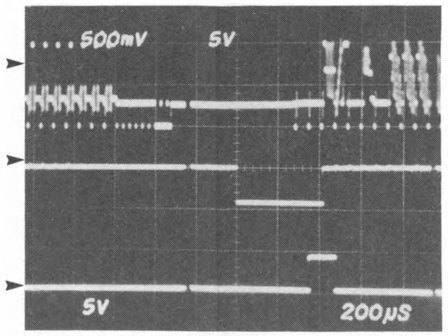
N

THIS TRACE IS VIDEO INPUT PWA 3 TP1

U58-13
QUALIFY VCO LOCK — WF22

TP11
RESET QUALIFY — WF18

TRIG: TP11, VPR IN NORMAL PLAY, SYNC HEAD OFF



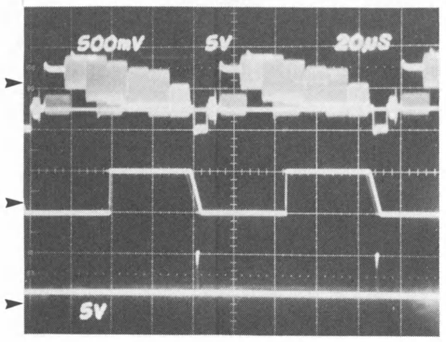
O

THIS TRACE IS VIDEO INPUT PWA 3 TP1

TP3
SEARCH ERROR RAMP — WF23

TP4
SEARCH SAMPLE PULSE — WF24

TRIG: TP4 VPR IN REWIND



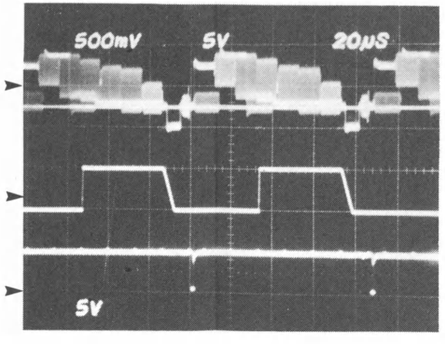
P

THIS TRACE IS VIDEO INPUT PWA 3 TP1

TP3
SEARCH ERROR RAMP — WF23

TP9
SEARCH 1365 — WF25

TRIG: TP4, VPR IN REWIND AS IN PHOTO ABOVE



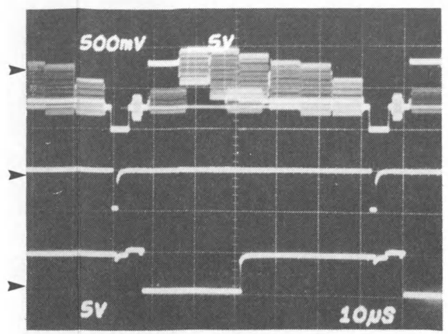
Q

THIS TRACE IS VIDEO INPUT PWA 3 TP1

PIN 49
FLYWHEEL SYNC — WF9

PIN 23
VCO WRITE PULSE — WF10

TRIG: PIN 49



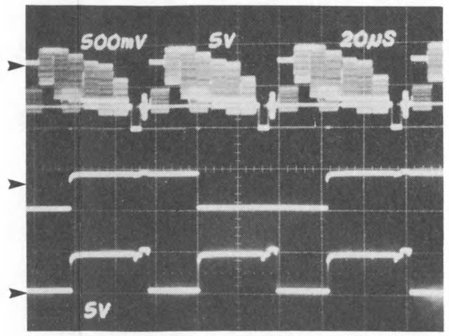
R

THIS TRACE IS VIDEO INPUT PWA 3 TP1

PIN 23
VCO WRITE PULSE — WF10

PIN 84
FLYWHEEL SYNC — WF11

TRIG: PIN 34



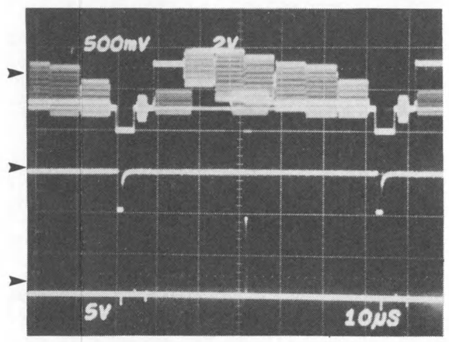
S

THIS TRACE IS VIDEO INPUT PWA 3 TP1

PIN 49
FLYWHEEL SYNC — WF9

PIN 27
1/2 LINE — WF12

TRIG: PIN 27



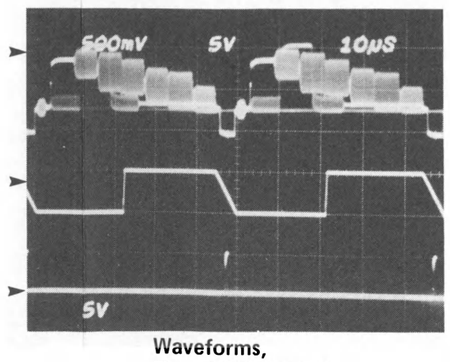
T

THIS TRACE IS VIDEO INPUT PWA 3 TP1

TP3
SEARCH ERROR RAMP — WF23

TP4
SEARCH SAMPLE PULSE — WF24

TRIG: TP4 VPR IN FAST FORWARD—NEARLY 300 in/s



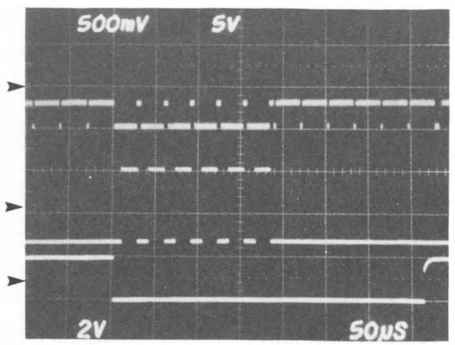
U

THIS TRACE IS VIDEO INPUT PWA 3 TP1

PIN 57
TAPE VERTICAL — WF13

PIN 33
PB VERTICAL — WF14

TRIG: TP11, VPR IN NORMAL PLAY, SYNC HEAD ON



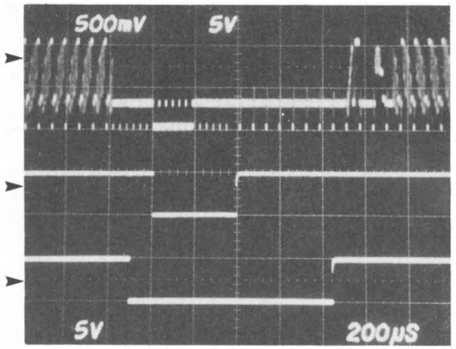
V

THIS TRACE IS VIDEO INPUT PWA 3 TP1

PIN 33
PB VERTICAL — WF14

PIN 69
HEAD SWITCH
V DROPOUT — WF15

TRIG: TP11, VPR IN NORMAL PLAY, SYNC HEAD ON



Waveforms,
Tape VCO PWA 6
REFERENCE 6

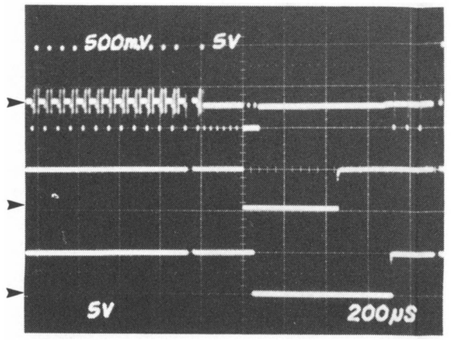
W

THIS TRACE IS VIDEO INPUT PWA 3 TP1

PIN 33
PB VERTICAL — WF14

PIN 69
HEAD SWITCH
V DROPOUT — WF15

TRIG: TP11 VPR IN NORMAL PLAY, SYNC HEAD OFF



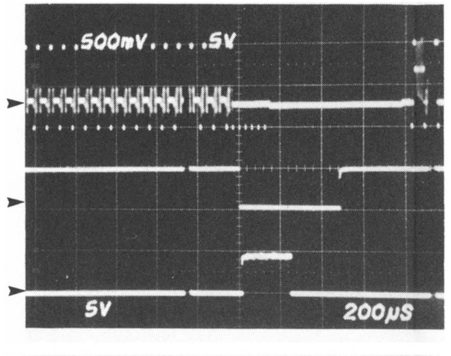
X

THIS TRACE IS VIDEO INPUT PWA 3 TP1

PIN 33
PB VERTICAL — WF14

PIN 32
VCO VERTICAL — WF16

TRIG: TP11, VPR IN FREEZE, SYNC HEAD OFF

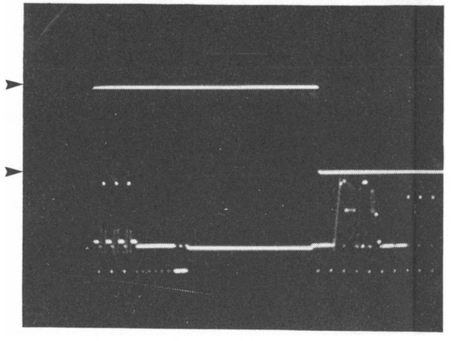


Y

TP10
VERTICAL INHIBIT — WF25

THIS TRACE IS VIDEO INPUT PWA 3 TP1

TRIG: TP10, VPR IN PLAY, SYNC HEAD OFF. R88 SET FOR START OF CORRECTION AT SECOND H FOLLOWING V INTERVAL.



PWA 6 Adjustable Components

COMPONENT	FUNCTION
L1	Normal oscillator
L2	Frequency error
R21(1)	Search oscillator test
R45	Tape-H reset and qualify delay
R50(2)	VCO phase comparator range
R53	H-sync phasing
R88	Vertical delay
R143(1)	Down VCO range
C20(1)	Up VCO trim

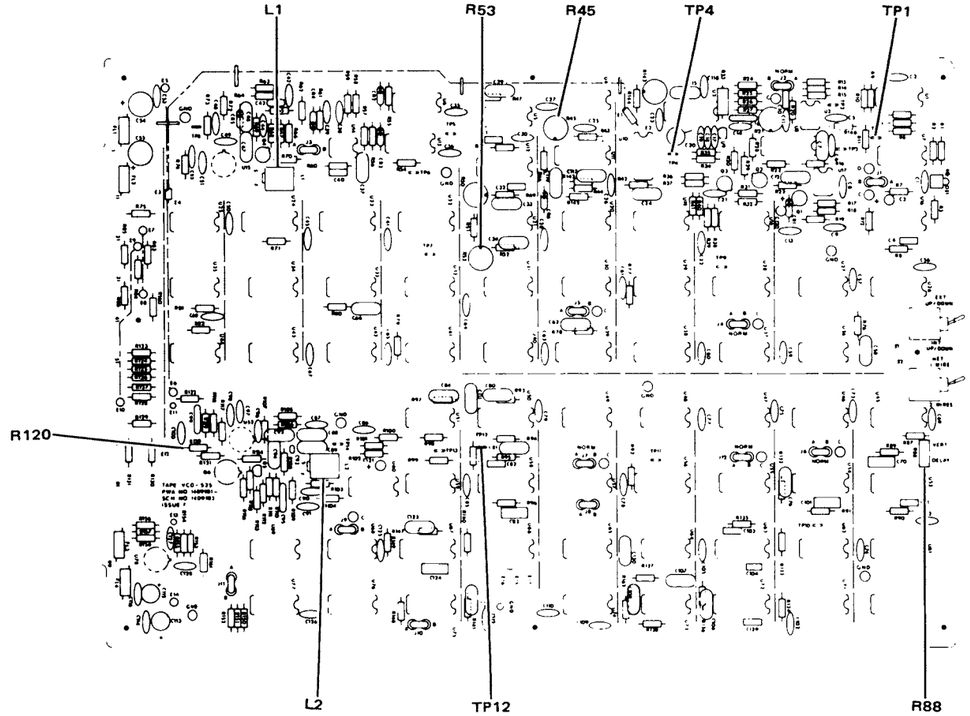
(1) Factory adjust only.
(2) R50 is adjusted for a 50% duty cycle at U12-13 with a 10–12V random error input (an active factor only when VCO is accessing new video).

PWA 6 Test Points

TEST POINT	FUNCTION
TP1	+4 volts VCO error voltage
TP2	Search oscillator control
TP3	Search error ramp
TP4	Search sample pulse
TP5	Gated tape H reset
TP6	H-rate reset
TP7	Tape-H reset
TP8	6 Fsc
TP9	Search reset—1365
TP10	Vertical inhibit
TP11	Vertical reset qualify
TP12	Qualify pulse
TP13	Tape pulse
TP14	1/2 subcarrier oscillator error

PWA 6 Jumpers

JUMPER	POSITION – FUNCTION	
J1	A–B	Normal
	B–C	Forces search condition
	B–D	Forces normal condition
J2	A–B	Normal
	B–C	Inserts test voltage for search oscillator
J3	A–B	Normal
	Removed	Removes error to normal oscillator
J4	A–B	Normal, remote selection of up/down oscillator
	B–C	Auto selection of up/down oscillator
J5	A–B	Normal
	B–C	Test – forces VCO phase comparator
J6	A–B	Single-wire heterodyne operation
	B–C	Two-wire heterodyne operation
J7	A–B	Normal
	B–C	Test – defeats H reset
J8	A–B	Normal
	Removed	Test – verifies reset qualify counter
J9	A–B	Sync head video processing
	B–C	Normal
J10	A–B	Normal
	Removed	Disables tape vertical to vertical delay
J11	A–B	Normal
	Removed	Disables VPR vertical to vertical delay
J12	A–B	Back porch dropout operation
	B–C	Front porch dropout operation



PWA 6 Component Locator

PWA 6 Component Locator

SECTION 7

MEMORY CONTROL
DESCRIPTION AND MAINTENANCE

7-1. INTRODUCTION

Refer to the following documents in the *Parts Lists and Schematics* manual:

ASSEMBLY No. 1409094

SCHEMATIC No. 1409096

Numbered data sheets (REFERENCE 1, 2, 3 . . . *n*) to which PWA descriptions and maintenance procedures refer are located at the end of this section as follows:

Overall Block Diagram – REFERENCE 1

Simplified Schematic – REFERENCE 2, 3, 4, 5

Waveforms – REFERENCE 6, 7, 8

Maintenance Data – REFERENCE 9

MEMORY CONTROL PWA 7
FUNCTION SUMMARY

- Write control is synchronous to tape 3.58-MHz timing and provides:
  a. Memory board address and line select addressing for main memory and velocity compensator line error store.
  b. Separate two-phase write clocks for main and dropout memory.
  c. Three phases of 10.7 MHz for 8-to-24-bit serial-to-parallel conversion on PWA 9.
- Read control is synchronous to reference video 3.58-MHz clock (modulated by velocity compensator) and provides:
  a. Memory board address and line select addresses for main memory and velocity compensator line error store.
  b. Two-phase memory read clocks (modulated by vel comp).
  c. Three phases of 10.7 MHz for 24-to-8-bit parallel-to-serial conversion on PWA 13.
  d. Reference 10.7-MHz clock for D/A conversion on PWA 14.
- Memory centering and overload logic maintain the relationship of read-to-write addressing within the center of the correction range:
  a. A write overload condition (tape slow compared to reference) enables the dual load which advances write address two lines and simultaneously loads the skipped line (resulting in two lines of video repeated).
  b. A read overload condition (tape fast compared to reference) inhibits the write address counter from incrementing for two lines and inhibits writing for two lines (two lines of video are dropped).

7-2. DESCRIPTION

The Memory Control PWA generates control signals that regulate the flow of digitized video through the TBC. Write control signals are clocked by 3 Fsc (10.7 MHz) which is phase-locked to the tape burst crossing and the leading edge of tape H sync. The write function is initiated by the write pulse from the Tape H Comparator PWA which occurs just after the color burst on the back porch of horizontal blanking. Read control signals are clocked by reference H-drive from the Sync Generator PWA, which is in phase with the reference Fsc. Because these signals are timed to broadcast standards, digitized video read out of memory will be time-base corrected for any errors due to the tape or the playback process.

Memory Control PWA 7 is divided into three general circuit areas: write timing, read timing, and line and field registration as shown on the REFERENCE 1 block diagram.

As illustrated in Figure 7-1, TBC Data Flow Block Diagram, Memory Control may be regarded as the center of a control system that moves digitized 8-bit data representing input video from the A/D Converter PWA at 3-Fsc rate into the Serial-to-Parallel Converter PWA. There it is assembled in a 24-bit register and shifted at Fsc rate into the memory. As data is written into a given line of memory, a previously written line is read out at reference Fsc rate into the Parallel-to-Serial Converter PWA. There it is latched and read out to the Video Out PWA at reference 3 Fsc rate. During the process of moving data from Memory to the Video Output PWA, the Sync Generator PWA further refines time-base correction (if the velocity compensation option is installed) by providing a modulated reference 3 Fsc to correct for errors introduced by the tape head crossing the vertical dropout gap.

Line and field registration circuits perform three primary functions: (1) to servo the relationship between the line being written into memory at a given time and the line being read out of memory to a six-line difference (i.e., read line 1 paired with write line 6) (see Figure 7-2, Read/Write Time Relationship), (2) to servo the video frame into registration with the "top" of the television screen, while maintaining the six-line read-write difference; the vertical centering function may be selected by a switch at the front edge of the Memory Control PWA, and (3) search mode permits picture display on the monitor during shuttle operation of the playback mechanism.

7-3. Write Timing

Write timing circuits perform two primary functions: (1) timing of data from the A/D Converter into the Serial-to-Parallel Converter, and (2) timing of data from the Serial-to-Parallel Converter into the memory. They also provide signals for the slow-motion function during editing, and a signal to invert the phase of the chroma at the frame/2 (color frame) rate. Write timing may be modified by: (1) vertical centering of the field, (2) memory centering of data in storage, (3) correction required during editing.

Write-pulse reclocking flip-flops serve to insure that the 3-Fsc pulse that clocks the serial-to-parallel shift register, write shift pulse clock, and reset counters is synchronous with the write pulse. The reclocked write pulse initiates action in these circuits at the start of the data line by presetting serial-to-parallel shift registers to WCB3. The next 3-Fsc pulse shifts the circuit to WCB1; reset counters are enabled and write shift clock pulses are initiated.

7-4. Memory Write Control. The principal clock for the line address counters (WA0, WA1) is the delayed flywheel sync. (See REFERENCE 1, Memory Control Block Diagram, and Write Control Waveforms O, P, Q, and the simplified schematic, REFERENCE 3.) WA0 and WA1 with the appropriate board select signal (WMA, WMB, WMC) will enable the write gates of each of 12 lines of memory in sequence. WA1 is also used as the clock for the shift register which generates the WMA, WMB, and WMC intervals. WØ1 and WØ2 are two phase clock pulses used by the memory to shift data into storage at the tape Fsc rate. Write clock reset is used by the Memory PWA to reset the write shift enable latch at the end of each line of data. Reset counters are started by the delayed write pulse at the end of the horizontal blanking period. At this time the WM board select output gates are enabled. The reset counters permit 199 words of data to be entered into a given line of memory. At the end of this event the output gates are inhibited, thus closing the write gates in memory. Shift pulses continue to a count of 255, resulting in a shift of 55 words of zero value bits into the memory line behind the data. A total of 254 shifts have been made. The memory line is 256 words in length, therefore the two "forward" registers at the output end are also zero value words. Since all memory lines on a given board are wire-OR'ed at the outputs, the two "extra" zero value words serve to prevent mixing of data from two or more lines.

7-5. Serial-to-Parallel Converter Write Control. The serial-to-parallel shift registers generate the WCB1, WCB2, and WCB3 intervals. (See write control waveforms L and M.) This signal controls

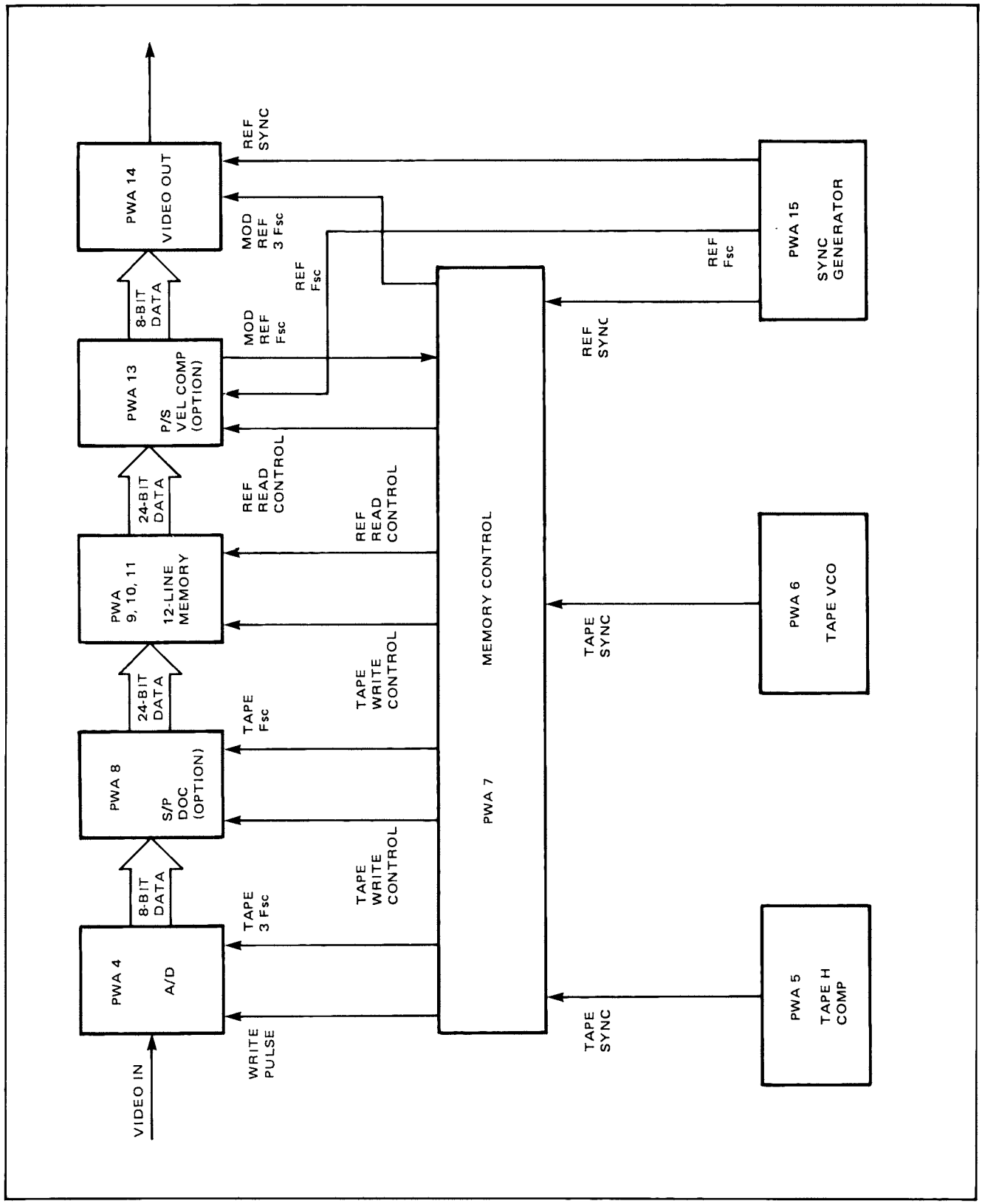


Figure 7-1. TBC-2 Data Flow Block Diagram

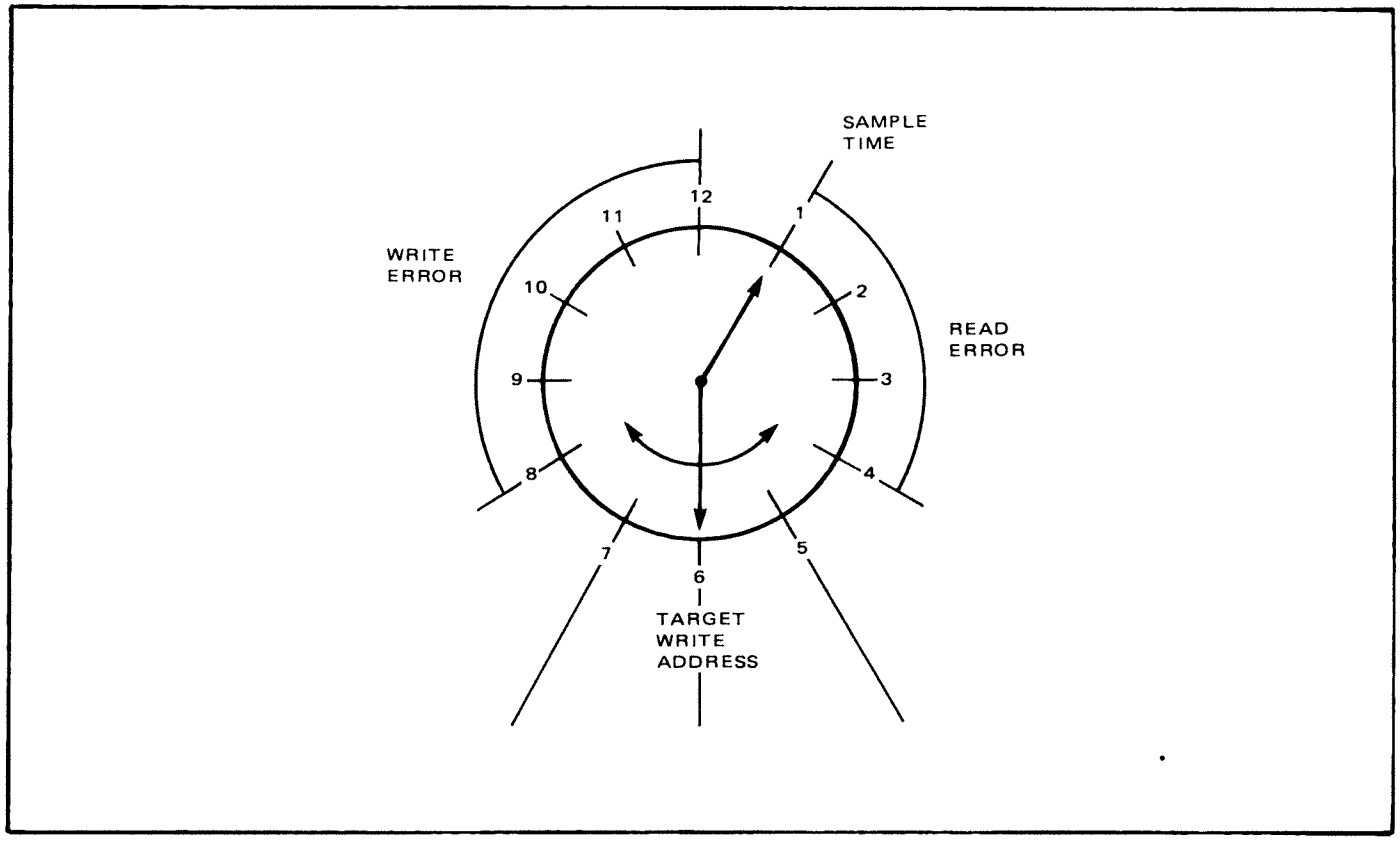


Figure 7-2. Read/Write Time Relationship, Memory Control PWA

the loading of data into the Serial-to-Parallel Converter PWA 8 in 8-bit groups (luminance video level sample) and transfers them into a 24-bit word in the output latch. If the Serial-to-Parallel Converter PWA has the dropout compensation option, control signals WMA, WMB, WMC–WA0, WA1–DCϕ1, DCϕ2 – and terminate clock are also used.

7-6. Read Timing

Reference subcarrier (chroma phase component) from the sync generator is the source of read timing. If the velocity compensator option is installed, velocity-compensated read Fsc at pin 82 from PWA 13 becomes the basic source timing for memory read, P/S conversion, and the D/A conversion on the Video Output PWA. This read Fsc is a 3.58-MHz pulse train which varies in phase as a function of the velocity line error. Reference H drive at pin 72 which is the source for the read stop/start timing for each line in memory is reclocked by read Fsc to establish the registration of the left picture edge. The read start of the picture data is adjusted in 140-nanosecond increments by the horizontal phasing digital switch on the Memory Control PWA edge. The read timing can be followed on the simplified schematic of REFERENCE 2 and the read control waveforms are given on REFERENCE 6 (Waveforms A–K).

7-7 P/S Converter Read Timing. Velocity compensator circuits on PWA 13 require the same line-by-line read timing as the memories so that the read Fsc output of PWA 13 is synchronous with the line being read out of memory. The clock circuits reclock the delayed H phase pulse to synchronize with the 3-Fsc rate. The reclocked pulse resets the parallel-to-serial shift register to RCB3 and enables the 224-bit counter. The next WCB1 signal triggers the pulse generator starting the count and the Rϕ1, Rϕ2 shift pulse

clock. After 224 read shift pulses, the carry output of the counter resets the enable flip-flop and the circuits wait for the next reference H-drive pulse. RCB1 and RCB2 operate the 24-bit latch and multiplexer of the Parallel-to-Serial Converter PWA 13.

7-8. Memory Read Control. Line address counters are reset by the 7.8-kHz/Reference V/2 color frame one-shot and clocked by H-drive to develop RA0. RA1 clocks the RM board select shift registers. Rϕ1 and Rϕ2 shift data from the memory to the Parallel-to-Serial Converter. RMC, RA1 and RA0 are also used by the velocity compensation option in the parallel-to-serial converter.

The reference 7.8 kHz is the D-input to the color frame rate counter. Reference V/2, which occurs at video frame rate, clocks the counter at the end of the first sequence of F/4 counts. A pulse is generated which presets the line address counter to line 3 and the RM board select shift register to RMA. At 2,100 lines or four frames later, the pulse at TP3 is repeated. Since the 12 lines of memory are evenly divisible into 2,100, all pulses after the first one should find the preset condition already present. F/4 and F/2 with ADV V/2 are sent to the line and field registration circuitry to generate vertical strobe.

7-9. Write/Read Registration Decode

See REFERENCE 4 and REFERENCE 5 for simplified schematics and waveform callouts for the memory centering circuitry. The write/read registration decode is used in two modes, search and centering. In the vertical centering or memory centering mode, search inhibits the read/address to the multiplexers. Therefore, the multiplexer becomes a write address decode. The clock signal from the latch clock generator, although encoded with RA1–RMC, actually occurs at the beginning of RA1–RMA (line 1) due to calculated delays in the delayed flywheel sync. Thus, whatever line of memory is being written into *at that time* will be latched for 12 lines of operation. The latched write address is decoded to the specific line in the 2-line to 4-line multiplexers. The one line of 12 selected will go low and the appropriate LED will light up. The green LED, DS7, is the "target" of the system. Illumination of a red light is an indication of a read/write registration error, which will cause the registration error decode to advance or retard the write clock plus or minus two lines to bring the system back into registration.

7-10. Registration Error Decode. Lines 1–5 and 7–12 of the write/read registration decode are inputs to the error decode gates. Lines 1 OR 2 *or* lines 11 OR 12 will, if one goes low, preset the error delay counter to 14 and only one pulse will be required for the carry signal to clock the error signal from the error decode gates into the appropriate sample-and-hold JK flip-flop. Lines 1 OR 2 *or* 3 OR 4 are decoded as an error signal to the read digital sample-and-hold flip-flop. Lines 8 OR 9 *or* 10 OR 11 are decoded as an error signal to the write sample-and-hold flip-flop. However, if the error is confined to the 3, 4, 8, 9, 10 area, the counter will not be preloaded and the counter must count to 15 (60 lines) before the error is clocked into the sample-and-hold flip-flop.

The decode clock produces a signal which is in phase with, but approximately 1 microsecond in advance of, WA1. When ADV WA1 goes high (end of line 2), the clock is advanced. When the carry is generated the error is clocked into the sample-and-hold flip-flop. When ADV WA1 goes low a 1.5-microsecond delay triggers the appropriate one-shot to produce either a plus-two-line-signal or a minus-four-line signal and a plus-two-line signal. Lines 1, 2, 3, and 4 from the registration decode are designated as read error signals and will produce a plus-two-line pulse (advance two lines) and a dual load. Dual load will load identical data into lines 3 and 1, and lines 4 and 2. Lines 8, 9, 10, 11, and 12 are designated as write error signals and will produce a minus four-line signal and a plus-two-line signal (retard two lines).

When the plus-two-line pulse is generated, WA 1 is preset to the lines 3 and 4 condition. Thus, lines 1

and 2 of the sequence following the advance two-lines signal are deleted, and the "empty" lines 1 and 2 are written with "pseudo" video (contents of lines 3 and 4) by the dual load to eliminate a two-line white streak.

When the minus-four-line pulse is generated, the WA1 "clock" to the WM board select shift register is blocked, holding the shift register in its mode of the moment. The plus-two-line pulse operates as previously described, with a resultant retard of two lines. This could be regarded as an instruction to "rewrite lines 3 and 4 with current data."

If the tape H rate is such that the write address sampled by the registration decode latch falls within the read error area (lines 1, 2, 3, or 4), a plus-two pulse and $\overline{\text{dual load}}$ will be generated to advance the write address toward a six-line read/write address difference. Because the write address is sampled at read line 1 address time, the "target" of the write address is write address 6. After 12 successive lines of memory read, the write address is sampled again, and if error is found, the write address will be advanced two more lines. This process will continue until the write address falls within the write 5, 6, or 7 address area.

If the write address falls within the write error area (lines 8, 9, 10, 11, or 12) the minus four and plus two pulses will retard the write address two lines. This action will continue, in 12 memory read line intervals, until the write address falls within the write 5, 6, or 7 address area. The write/read registration decode, registration error decode, latch clock generator, and write address circuitry comprise a digital servo system.

7-11. Vertical Strobe Generator. At the start of every fourth frame the read address is preset to line 3-RMA. If a six-line read/write address difference is maintained, the write address will be line 8 (line 4-RMB). Tape vertical sync is offset in respect to the start of the vertical interval so that at the 10th line (start of the back porch of the vertical interval) the address will be: read line 1, write line 6. The function of the vertical strobe generator is to enforce this condition, and thereby align the top edge of the picture on the screen.

If the vertical/memory centering switch is in the vertical position, the vertical strobe generator is enabled. While the counter in the strobe generator circuitry is counting (4.9 ms) the latch clock generator is disabled.

In the eighth field of the F/4 signal, F/2, F/4, and ADV V/2 are AND'ed to preset a JK flip-flop and $\overline{Q}$ goes low. The first flywheel sync pulse at tape vertical will clock the JK and $\overline{Q}$ goes high. Since the preset was made by a combination of signals from reference V/2 and reference 7.8 kHz, and the reset was established by signals from the tape, the width of the pulse at $\overline{Q}$ is a measure of the phase difference between the two vertical rates. When $\overline{Q}$ goes high the counter is enabled and is clocked by flywheel sync. After 13 counts the 64-bit is high and will remain for 64 more counts (total 77). After the 77 count the carry pulse locks the vertical strobe circuits until another F/4-field 8 pulse presets the JK to start the process again.

The leading edge of the vertical strobe clocks the latch of the write/read registration decode. The latched write address is held for the duration of the vertical strobe. If an error is decoded the write address will be servoed toward the line 5, 6, 7 area. When a line 5 or 7 error is decoded, a secondary circuit latches the error on the trailing edge of the vertical strobe. Another counter is enabled and is clocked by the trailing edge of the vertical strobe. After eight counts (32 frames) a slow centering pulse is OR-gated into the WA0 counter advancing the write address one line. The write address is therefore servoed to line 6.

Because the read address is preset to line 3 at the beginning of the frame and becomes line 1 at the 10th line of the vertical interval and the write address is servoed to line 6 during the vertical interval, the correct read/write relationship is established at the beginning of the frame.

When the vertical strobe generator is locked out at the end of the strobe the latch clock generator is enabled and centering continues to enforce the servo condition.

7-12. Search Mode. When in search mode (shuttle of the playback mechanism) the read addresses to the multiplexer in the write/read registration decode are enabled. The circuit then begins to commutate. Search also removes RMC as a condition for the latch clock and latch clock pulses are generated at each RA1-delayed flywheel sync interval. Therefore, the sampling rate is increased from one to 12 lines to one of four lines. Commutation of the address decode produces the following pattern:

MEMORY/ VERTICAL CENTERING	SEARCH			
	READ ADDRESS	RMA	RMB	RMC
Mux 1-A	Mux 1	A	B	C
Mux 2-B	Mux 2	B	C	A
Mux 3-C	Mux 3	C	A	B

The pattern produced by commutation will generate artificial error signals at a rate proportionate to tape speed multiplied by the increased sampling rate. The error signals thus produced will add or delete lines to maintain the correct number of lines of data loaded into memory. Although some lines may be deleted, or some may be loaded with false data, enough recognizable picture information is available to allow the operator to recognize the particular area of tape for which he is searching.

7-13. Interlace Select. During slow-motion editing by the playback mechanism, 1% (2-1/2 lines) of video information is "lost" in each field due to mechanical considerations. To compensate for this, the STEP BACK signal from the playback mechanism deletes alternately two or three lines from successive fields (average 2-1/2). Also, during this process the phase of the 3.58-MHz Fsc in the Color Processor PWA 2 must be reversed at the correct time in the color field. (See Waveforms V through AA.)

To delete the "lost" lines, two (or three) delayed flywheel sync pulses are OR-gated into the line address counters at reference vertical time. Thus, these lines are deleted before the field begins.

At the tape vertical time the even/odd comparator in the interlace select circuitry checks the relative position of delayed flywheel sync pulses and ADV V/2 to determine if the following field will be an even or odd number in the color field. During the time the "lost" lines are deleted, the even/odd signal is gated to the color processor.

7-14. MEMORY CONTROL MAINTENANCE

See REFERENCES 6, 7, 8, 9 in this section for the component locator diagrams and the jumper/test point/adjustable component summaries.

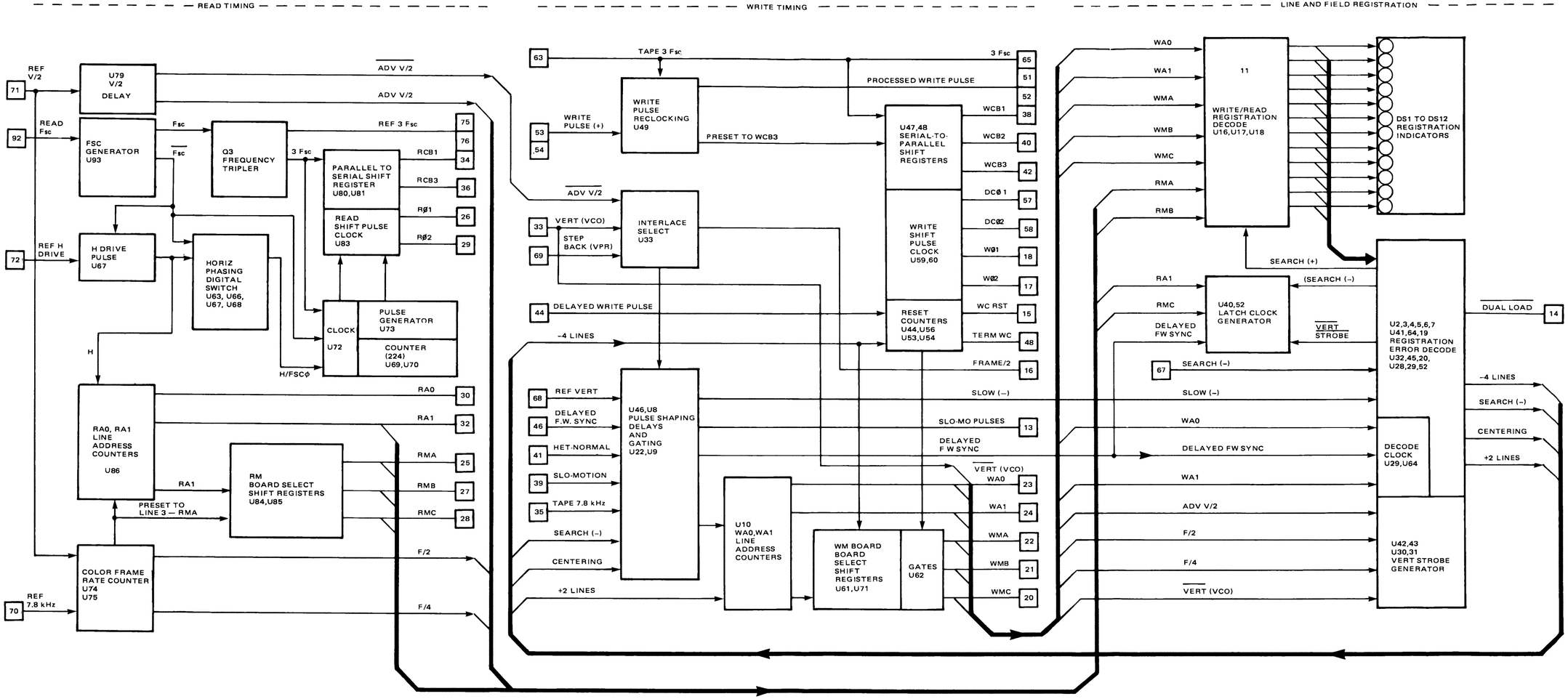
Before undertaking any adjustments to the Memory Control PWA, review the *System Alignment Guide* (Table 3-2) and the *Tape/Reference Test Loop* discussion (paragraph 3-5) in the *System Maintenance* section (Part I) for a general understanding of the scope of these field adjustments.

Consult REFERENCE waveforms and interconnect data on the simplified schematics to confirm normal operation of the Memory Control PWA and interactive functions between it and other PWA's before making any adjustments.

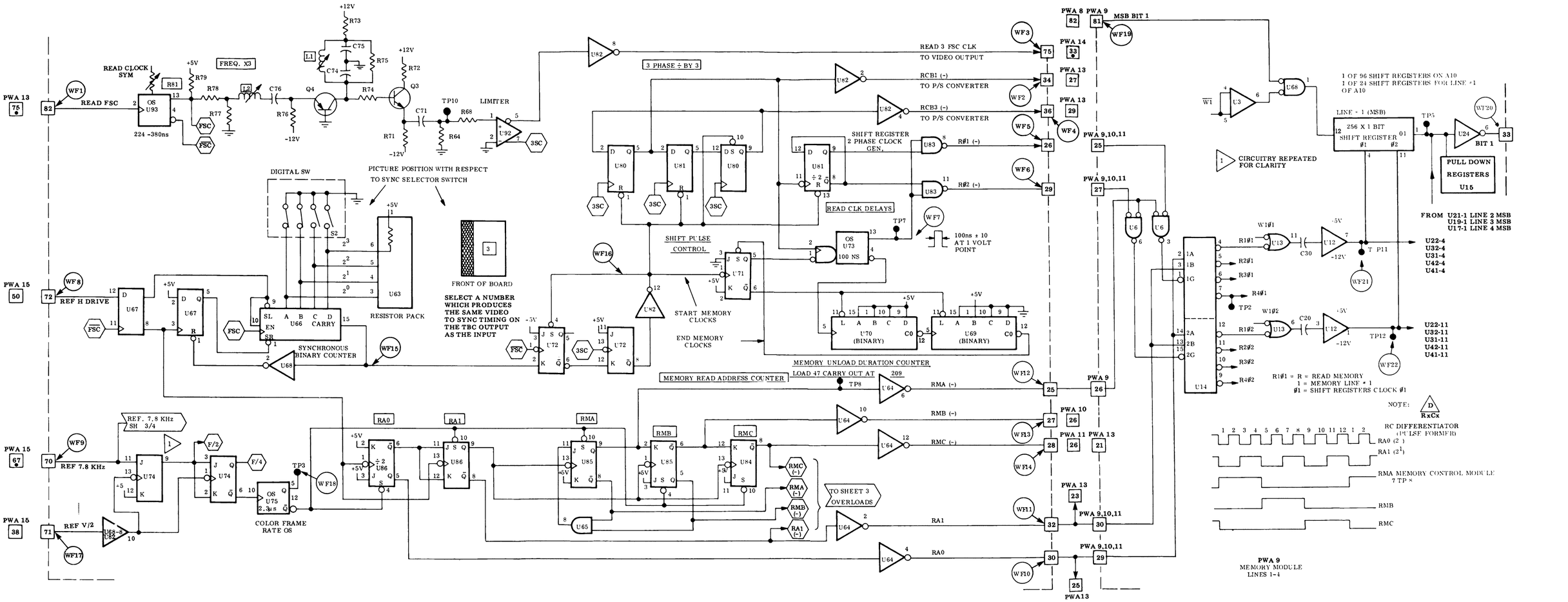
There are two adjustable functions on the Memory Control PWA. The first, S2 (H-video position), is part of the system level *Tape H/Sync to Video Timing* adjustment (paragraph 3-13).

The velocity-compensated reference subcarrier (read Fsc) is tripled and becomes the source for read clock timing of the Memory, P/S Converter, and Video Out PWA's. The adjustment insures a symmetrical reference 3 Fsc signal, and is accomplished as follows:

1. Use the tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN.
2. Connect oscilloscope to U93-13; trigger on internal.
3. Adjust R81 for a 50% duty cycle.
4. Connect oscilloscope to TP10 (3 X subcarrier); trigger on internal.
5. Adjust L1 (3 Fsc peaker) and L2 (3 Fsc filter) for maximum 3 Fsc – ranging between 1.5 and 4.0 Vp-p.

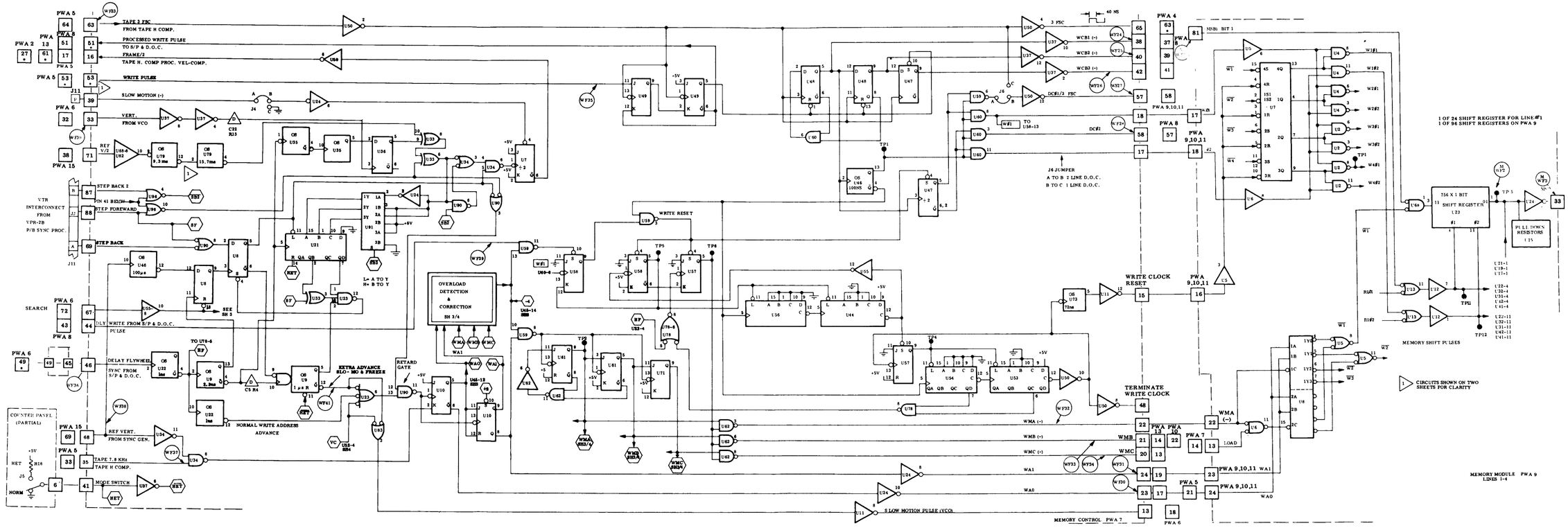


Memory Control
Block Diagram, PWA 7
REFERENCE 1

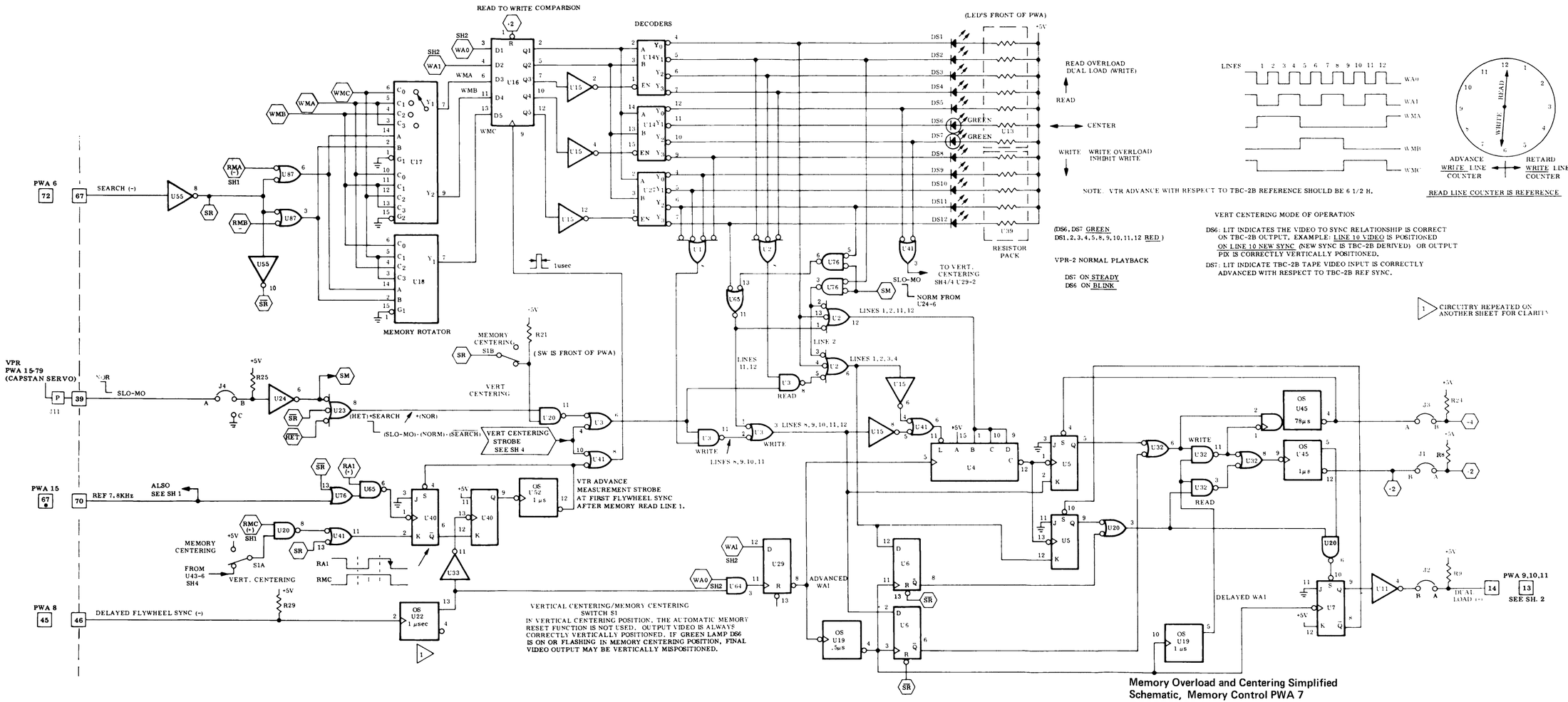


Read Control Simplified Schematic
Memory Control PWA 7
REFERENCE 2

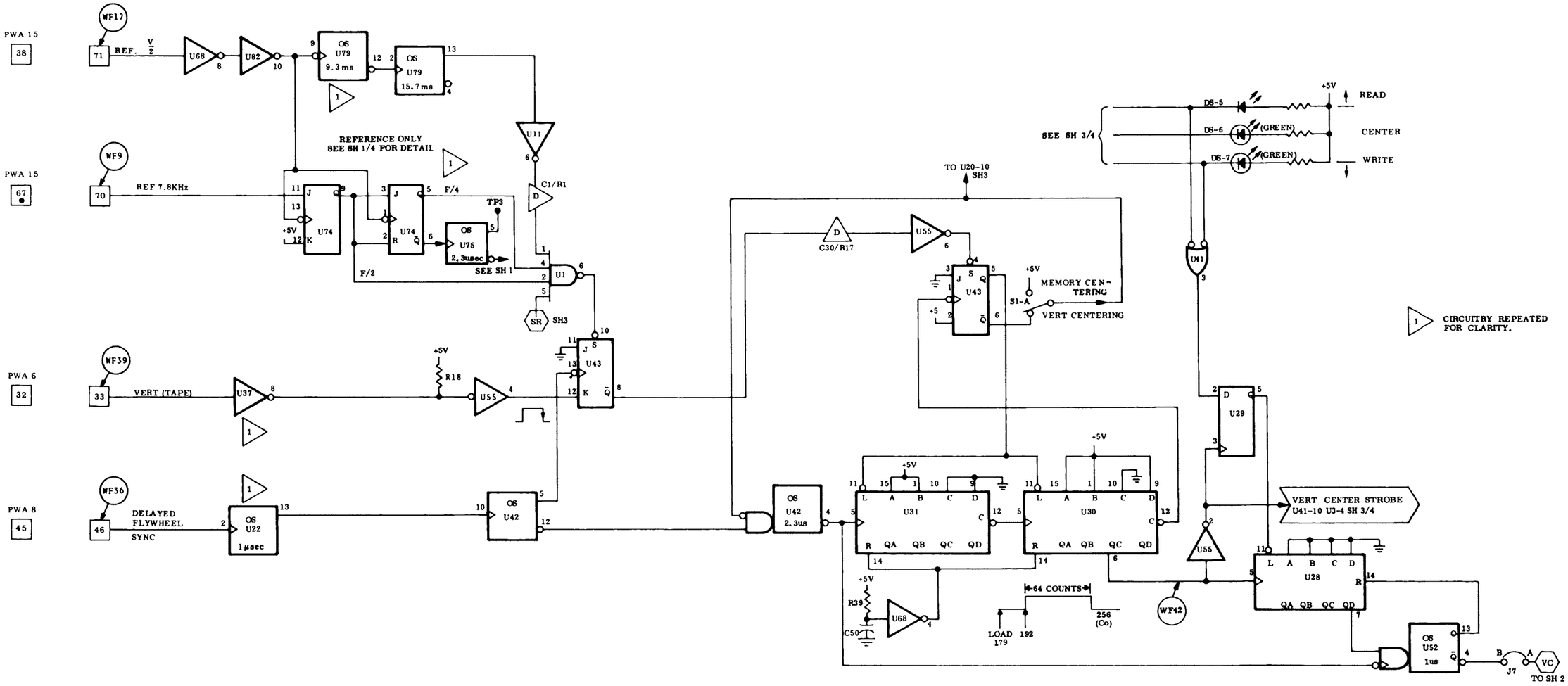
AMPEX 1809474-01



Write Control Simplified Schematic
Memory Control PWA 7
REFERENCE 3



Memory Overload and Centering Simplified Schematic, Memory Control PWA 7
REFERENCE 4



Memory Overload and Vertical Centering
Simplified Schematic, Memory Control PWA 7
REFERENCE 5

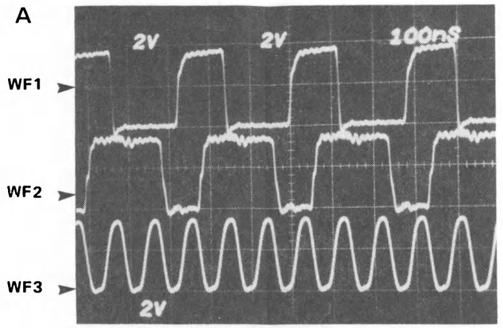
A

PIN 82
READ Fsc

PIN 34
RCB1

PIN 75
REF 3Fsc

TRIG: PIN 82



PIN 72
REF H DRIVE

PIN 70
REF 7.8 kHz

PIN 30
RA0

TRIG: PIN 70

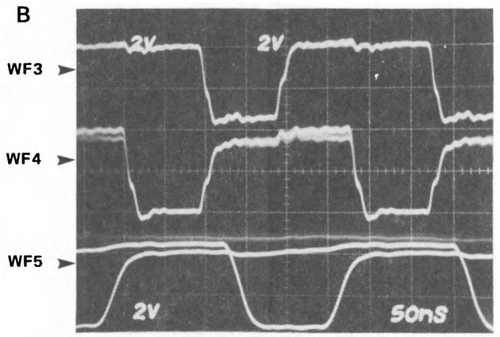
B

PIN 34
RCB1

PIN 36
RCB3

PIN 26
RØ1
NOTE TWO TIMING EVENTS

TRIG:PIN 34



PIN 30
RA0

PIN 32
RA1

PIN 25
RMA

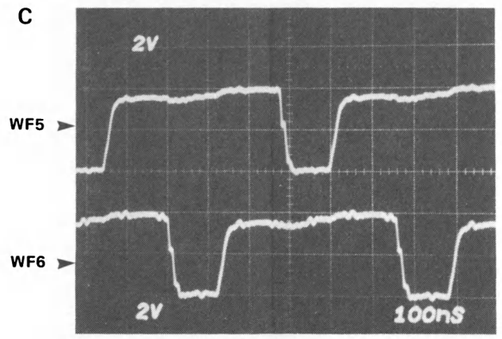
TRIG: PIN 25

C

PIN 26
RØ1

PIN 29
RØ2

TRIG: PIN 26



PIN 25
RMA

PIN 27
RMB

PIN 28
RMC

TRIG: PIN 28

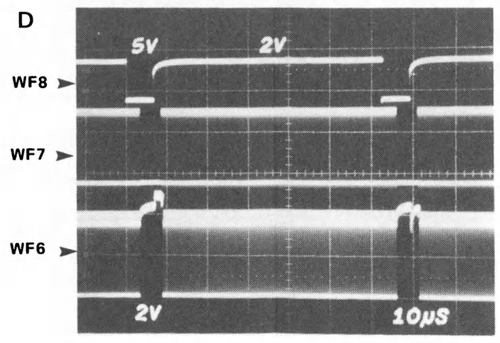
D

PIN 72
REF H DRIVE

TP7
READ CLOCK DELAY

PIN 29
RØ2

TRIG: PIN 72, DIGITAL SWITCH S2 SET TO 5



PIN 72
REF H DRIVE

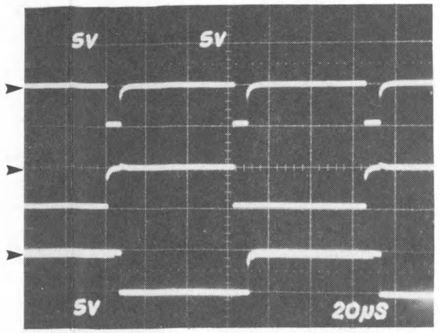
U66-15
DIGITAL SWITCH PULSE

U71-1
START MEMORY CLOCKS

TRIG: TP9

E

WF8
WF9
WF10



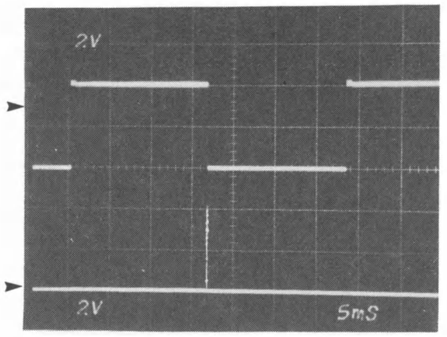
PIN 71
REF V/2

TP3 7.5 Hz RATE

TRIG: TP3

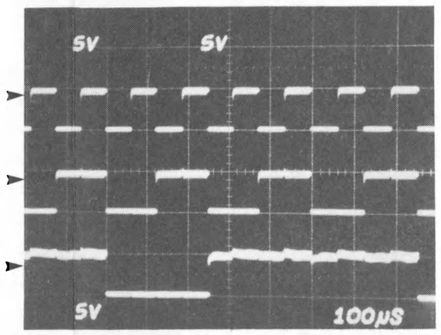
I

WF17
WF18



F

WF10
WF11
WF12



PIN 81
PWA 9

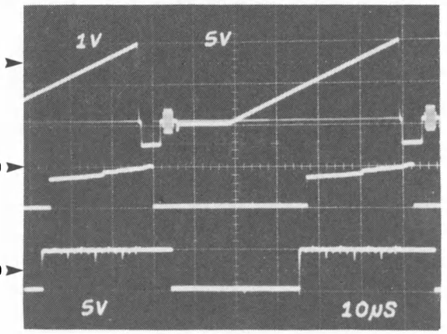
PIN 33
PWA 9

TRIG: PIN 33 TEST RAMP INSERTED FOR THIS PHOTO MODULE VPR IN E/E

J

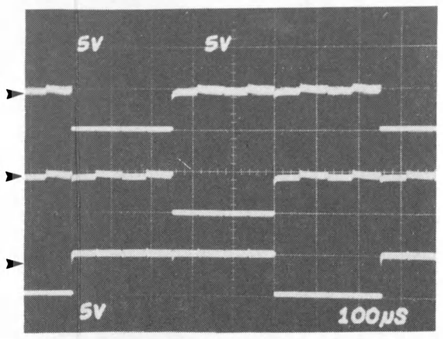
TBC VIDEO OUT 2

WF19
WF20



G

WF12
WF13
WF14



TP11
PWA 9

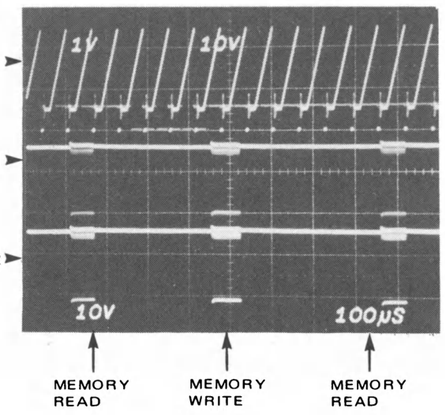
TP12
PWA 9

TRIG: PIN 26 PWA 9 VPR IN NORMAL "VERT" LOCK PLAY, UNITY TRACKING, TBC ADVANCE 6.5H LINES

K

TBC VIDEO OUT 2

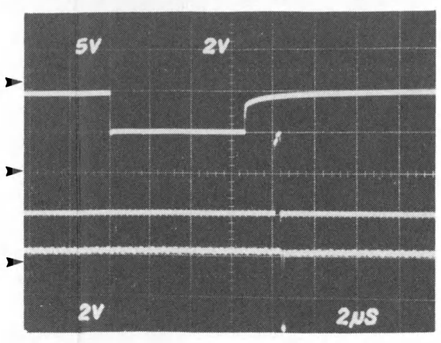
WF21
WF22



NOTE: START OF WRITE TO START OF READ IS 6.5H

H

WF8
WF15
WF16



Waveforms, Memory Control PWA 7
REFERENCE 6

AMPEX 1809474-01

L

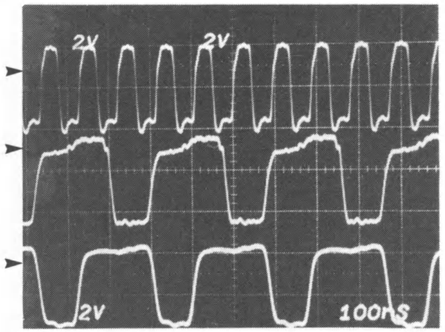
PIN 63
TAPE 3 Fsc

PIN 38
WCB1

PIN 40
WCB2

TRIG: PIN 40

WF23
WF24
WF25



PIN 23
WA0

PIN 24
WA1

PIN 22
WMA

TRIG: TP2

M

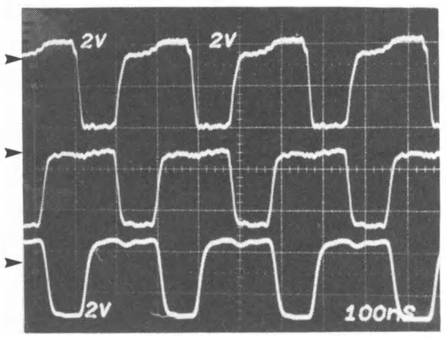
PIN 38
WCB1

PIN 40
WCB2

PIN 42
WCB3

TRIG: PIN 40

WF24
WF25
WF26



PIN 22
WMA

PIN 21
WMB

PIN 20
WMC

TRIG: TP2

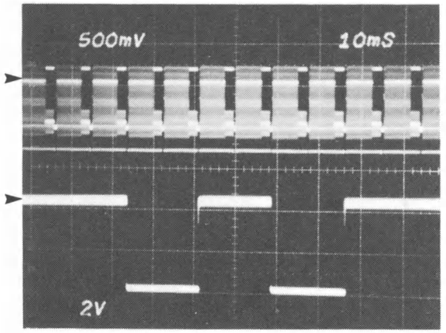
N

PWA 3 TP1
TAPE VIDEO IN

PIN 16
FRAME/2

TRIG: PIN 16.
VPR IN FORWARD SLO-MO

WF28



O

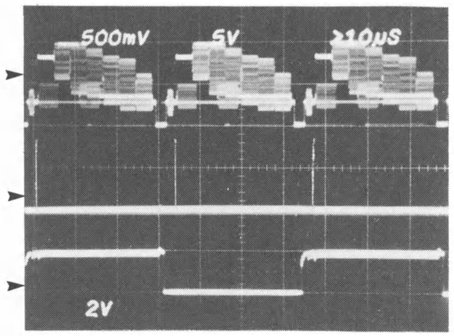
PWA 3 TP1
TAPE VIDEO IN

PIN 44
DELAYED
WRITE PULSE

PIN 23
WA0

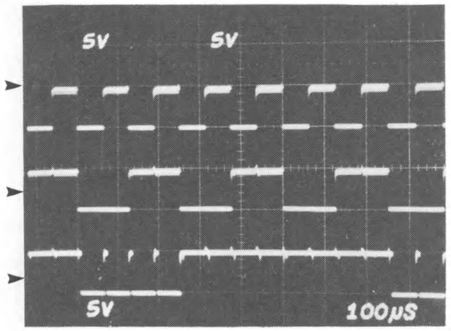
TRIG: PIN 44

WF29
WF30



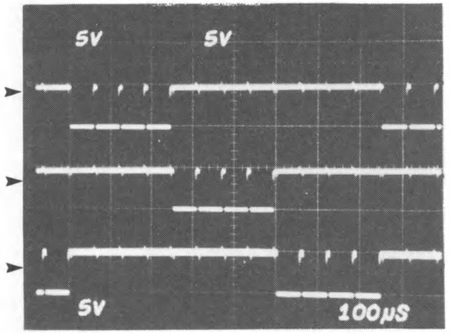
P

WF30
WF31
WF32



Q

WF32
WF33
WF34



R

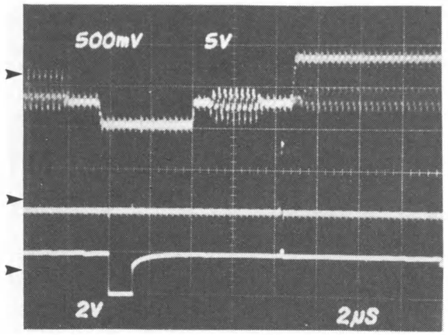
PWA 3 TP1
TAPE VIDEO IN

PIN 44
DELAYED
WRITE PULSE

PIN 46
DELAYED
FLYWHEEL SYNC

TRIG: PIN 46

WF29
WF36



S

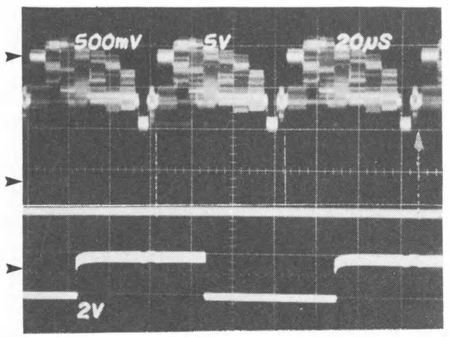
PWA 3 TP1
TAPE VIDEO IN

PIN 53
WRITE PULSE

PIN 35
TAPE 7.8 kHz

TRIG: PIN 35

WF35
WF37



T

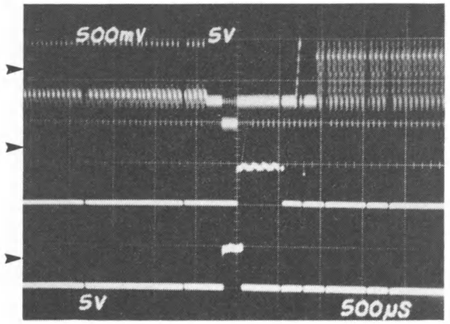
PWA 3 TP1
TAPE VIDEO IN

PIN 63
TAPE 3 Fsc

PIN 33
VCO VERTICAL

TRIG: PIN 68.
VPR IN E/E

WF38
WF39



U

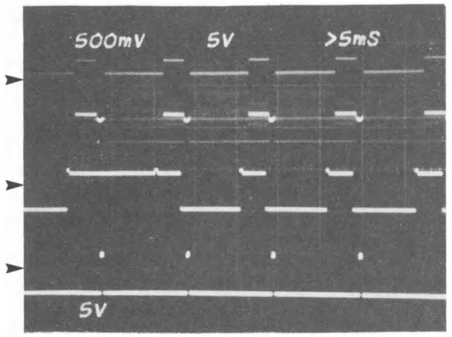
PWA 3 TP1
TAPE VIDEO IN

PIN 69
STEP BACK

PIN 68
REF VERTICAL

TRIG: PIN 68.
VPR IN SLO-MO≈1/4
SPEED

WF40
WF38



V

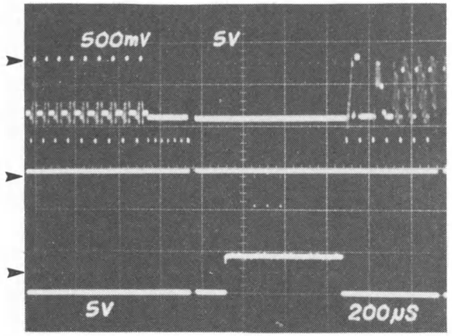
TBC VIDEO OUT 2

U9-12
ADVANCE

PIN 68
REF VERTICAL

TRIG: PIN 68.
VPR IN FREEZE

WF41
WF38



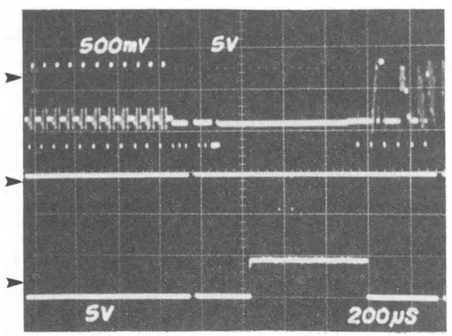
W

TBC VIDEO OUT 2

U9-12
ADVANCE

PIN 68
REF VERTICAL
TRIG: PIN 68.
VPR IN FREEZE

WF41
WF38



Waveforms, Memory Control PWA 7
REFERENCE 7

SLOW MOTION FORWARD— WAVEFORMS X AND Y

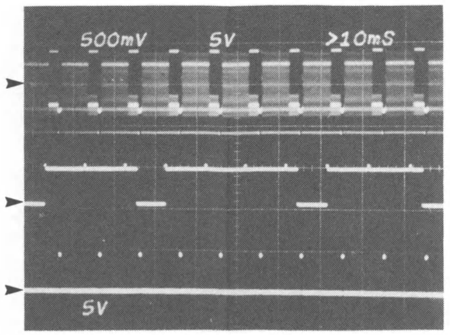
X

PWA 3 TP1 TAPE VIDEO IN

PIN 88 STEP FORWARD — **WF46**

PIN 68 REF VERTICAL — **WF38**

TRIG: PIN 88 VPR IN MAX SPEED (1 1/4X) SLO-MO FORWARD



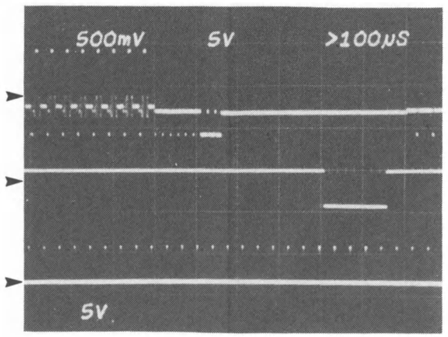
Y

PWA 3 TP1 TAPE VIDEO IN

U90-12 — **WF47**

U23-6 — **WF48**

TRIG: PIN 88 VPR IN MAX SPEED (1 1/4X) SLO-MO FORWARD



SLOW MOTION REVERSE— WAVEFORMS Z AND AA

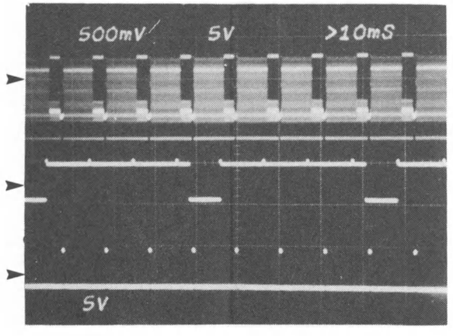
Z

PWA 3 TP1 TAPE VIDEO IN

PIN 87 — **WF45**

PIN 68 — **WF38**

TRIG: PIN 68 VPR IN REVERSE SLO-MO



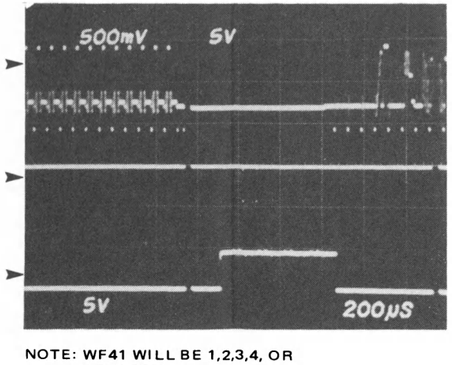
AA

PWA 3 TP1 TAPE VIDEO IN

U9-12 — **WF41**

PIN 68 — **WF38**

TRIG: PIN 68 VPR IN 1—1/4 SPEED REV SLO-MO



NOTE: WF41 WILL BE 1,2,3,4, OR 5 PULSES

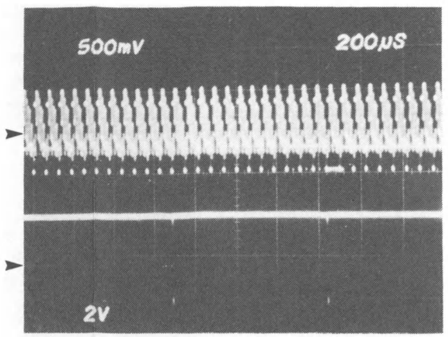
OVERLOAD— WAVEFORMS BB AND CC

BB

PWA 3 TP1 TAPE VIDEO IN

U41-9 — **WF50**

TRIG: U41-9 VERTICAL CENTERING/MEMORY CENTERING SWITCH TO VERTICAL CENTERING

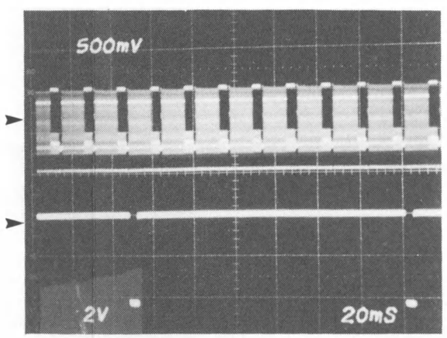


CC

PWA 3 TP1 TAPE VIDEO IN

U41-10 — **WF51**

TRIG: U41-10 VERTICAL CENTERING/MEMORY CENTERING SWITCH TO VERTICAL CENTERING



VERTICAL/MEMORY CENTERING IN VERTICAL FOR WAVEFORMS DD AND EE

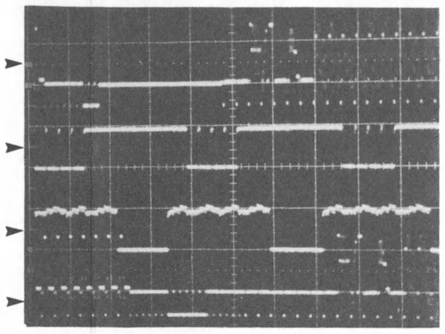
DD

PWA 3 TP1 TAPE VIDEO IN

PIN 22 WMA — **WF32**

PIN 25 RMA — **WF12**

TBC REF VIDEO
200 µs/cm HORIZ SWEEP
TRIG: TP3 VPR IN PLAY
6.5H ADVANCE, SYNC
HEAD OFF



NOTE: LINE 17 (VIT) IS BEING WRITTEN INTO LINE 6 OF MEMORY. WHEN MEMORY LINE 6 IS READ, MULTIBURST IS BEING PLACED IN LINE 17 OUTPUT SYNC.

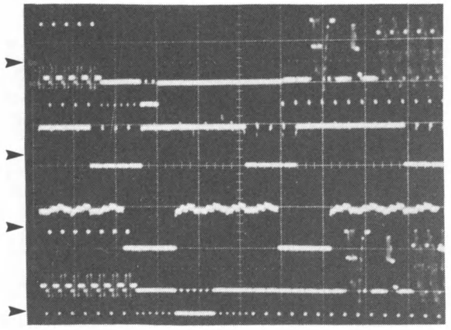
EE

PWA 3 TP1 TAPE VIDEO IN

PIN 22 WMA — **WF32**

PIN 25 RMA — **WF12**

TBC REF VIDEO
200 µs/cm HORIZ SWEEP
TRIG: TP3 VTR IN PLAY
2.5H ADVANCE, SYNC
HEAD OFF



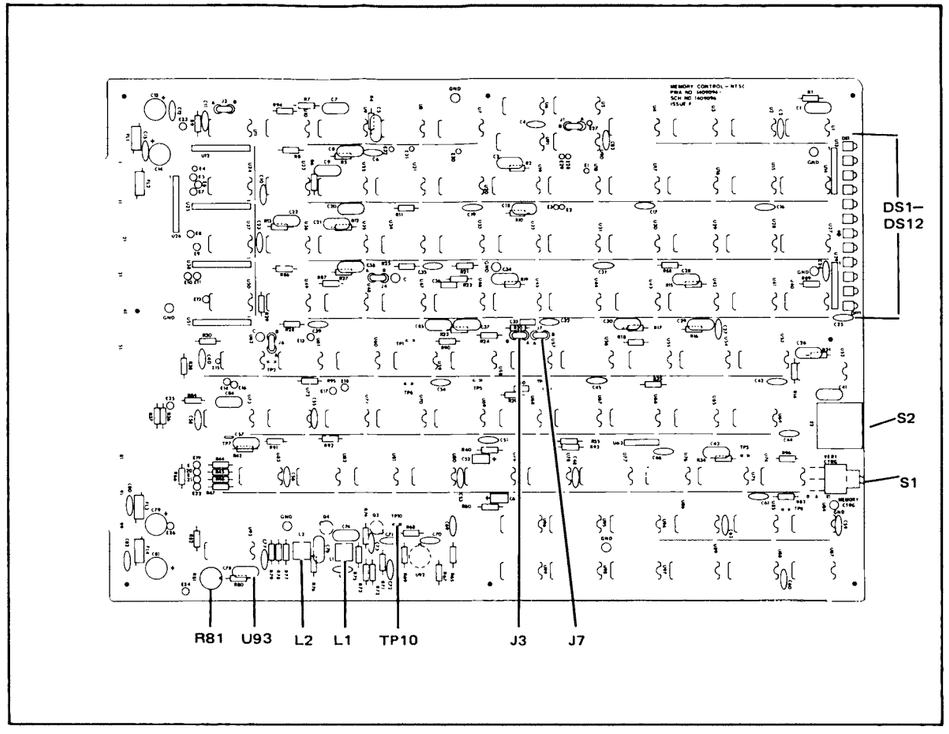
NOTE: OBSERVE THAT THE VTR ADVANCE HAS BEEN CHANGED FROM 6.5H TO 2.5H. HOWEVER, THE READ AND WRITE OF LINE 17 ARE UNCHANGED.

PWA 7 Test Points

TEST POINT	FUNCTION
TP1	100 ns pulse Fsc
TP2	Write memory A
TP3	F/4
TP4	H rate
TP5	H rate
TP6	Write enable
TP7	120 ns pulse at Fsc
TP8	Read memory A
TP9	(not used)
TP10	3 X subcarrier

PWA 7 Adjustable Components

COMPONENT	FUNCTION
L1	3 X subcarrier peaker
L2	3 X subcarrier filter
R81	Read clock symmetry
S2	H/Video position
S1	Memory/Vertical Centering



PWA 7 Component Locator

PWA 7 Jumpers

JUMPER	POSITION – FUNCTION	
J1	A–B Removed	Normal Test – disconnects over-load bus
J2	A–B Removed	Normal Test – disables dual load
J3	A–B Removed	Normal Test – disconnects over-load bus
J4	A–B B–C	Normal Test – forces slow motion
J5		(Not used)
J6	B–C A–B	Used with One-Line DOC (NTSC) Used with Two-Line DOC (PAL/SECAM)
J7	A–B Removed	Normal Test – inhibits write address from advancing

Test Points, Adjustable Components, Jumpers, Component Locator, Memory Control PWA 7
REFERENCE 9

SECTION 8

S/P CONVERTER (DOC)

DESCRIPTION AND MAINTENANCE

8-1. INTRODUCTION

Refer to the following documents in the *Parts Lists and Schematics* manual for the two versions of the S/P Converter:

One-Line DOC

ASSEMBLY No. 1409140

SCHEMATIC No. 1405132

S/P Converter Only

ASSEMBLY No. 1409122

SCHEMATIC No. 1402421

Numbered data sheets (REFERENCE 1, 2, 3 . . . *n*) to which PWA descriptions and maintenace procedures refer are located at the end of this section as follows:

One-Line DOC (1409140), Paragraph 8-2

Detailed Block Diagram – REFERENCE 1

Simplified Schematic – REFERENCE 2, 3, 4, 5

Waveforms – REFERENCE 5, 6, 7

Maintenance Data – REFERENCE 7

S/P Converter Only (1409122), Paragraph 8-14

Block Diagram and Maintenance Data – REFERENCE 8

S/P CONVERTER (DOC)
PWA 8 FUNCTION SUMMARY:

- Converts 10.7-MHz rate 8-bit data from A/D Converter B PWA 5 to 24-bit bytes at 3.58-MHz rate for entry into memory.
- Dropout compensator option continuously stores processed luminance and chrominance from two previous lines of the data flow for insertion into the data stream when a dropout is detected by the DOC control logic.

8-2. DESCRIPTION – ONE-LINE DROPOUT COMPENSATOR (1409140)

Dropouts are an undesirable occurrence in magnetic recording where short sections of the recorded signal are severely attenuated or missing. Fortunately, in video there is redundancy in the signal that can be used to disguise dropouts when they occur.

The TBC one-line DOC uses the substitution technique. In order to substitute information from the past, it must be stored in memory as it arrives from the tape. The TBC processes the video as luminance and chroma components, then reassembles these as composite video. Chroma is derived from two lines past and luminance from one line past. The simplified block diagram of Figure 8-1 illustrates the signal flow in the one-line compensation circuits. Note that the circuit blocks call out the appropriate simplified schematics from reference data at the end of this section.

8-3. Functional Description

See Figure 8-1 and REFERENCE 1. Video information from the A/D Converter PWA is latched by the input multiplexer and is designated as A-data to the digital luminance filter. Luminance is extracted by taking the average of three adjacent 10.7-MHz samples. The resulting luminance ($\overline{L}$) is subtracted from a delayed composite video word (V-data) which is the middle word of the three samples to obtain the chroma component, D-data. A complete line of D-data words is stored for a period of one

horizontal line in the RAM chroma memory. Data is read out of memory as C-data. C-data is added to L-data which has been delayed by two clock pulses to match the processing delay of the C-data. The L+C multiplexer checks the resulting composite video word for an overload condition. If an overload is detected for a given word a corrected word will be substituted in the multiplexer latch. The output of the latch, F-data, is stored in the one-line video memory for a one horizontal line period. Data is read out of the one-line video memory into the M-latch. Addressing of the data out of the memory is advanced by nine words to match the total processing delay of the data. Thus the M-data is in step with the data from the A/D Converter PWA. If a dropout is detected, data from the A/D Converter is blocked and M-data is substituted by the input multiplexer. Substitute data is sent to the serial-to-parallel converter circuit as A-data. If a multi-line dropout condition occurs, data stored in the dropout compensation memory is recirculated until the dropout condition terminates. In normal operation, incoming digital video data from the A/D is passed directly to the serial-to-parallel converter circuit and then to Memory PWA's 9, 10, and 11. The serial-to-parallel converter circuit of this PWA is identical in operation to the Serial-to-Parallel Converter PWA, Assembly No. 1409122, described below in Paratraph 8-14.

Recirculated data of a multi-line digital dropout compensation will deteriorate in quality on each iteration of a line. This is similar to the results obtained with analog delay lines. Contemporary high-quality tapes tend to have dropouts of 1/3 line or less in length; therefore, this effect is not usually noticeable.

The deterioration of quality in digital dropout compensation is primarily due to roundoff of the digital numbers in the processing of luminance and chroma data and the cumulative error resulting from recirculation of the data.

The output of the input multiplexer latch is designated as the A-data bus. The A-bus serves: (1) the serial-to-parallel converter, (2) the B-latch, and (3) the digital luminance filter. In the digital luminance filter, three successive samples of video data are added and divided by three to obtain the luminance value. (Luminance level is centered on the positive and negative peaks of the chroma signal; or conversely, chroma is centered on luminance.)

8-4. Digital Luminance Filter. See REFERENCE 2. The luminance filter adds the three samples of video and divides the value by 4. Further processing adds incrementally decreasing values until the final result is equivalent to a divide-by-3. The entire operation is a series of ADD – SHIFT RIGHT, ADD – SHIFT RIGHT, ADD, etc. operations. The sequence of events is as follows:

- Sum samples A and B. Carry in is 0. (U75/84)
- Divide result by 2, enter carry as MSB. (U57/50)
- Divide sample C by 2 and add to $\frac{A + B}{2}$. I-8 bit of C is carry in. (U58/67)
- Divide result by 2 and enter carry as MSB. (U49/50)
- Result is "S" value. $S = \frac{A + B + C}{4}$. (U49/50)
- Divide S by 4 and add to S. S-7 bit is carry in. (U39/48)
- Result is "P" value. (U40/14)
- P = (A + B + C) + (1/4 + 1/16)
- Divide P by 16 and add to P. Carry in is 0. (U32/23)
- Result is "L" value, or luminance. (U31/22)
- L = (A + B + C) + (1/4 + 1/16 + 1/64 + 1/256 = (A + B + C) + (85/256) = (A + B + C/3) to 8-bit accuracy.
- L-bar is the 1's complement of L. (U31/22)

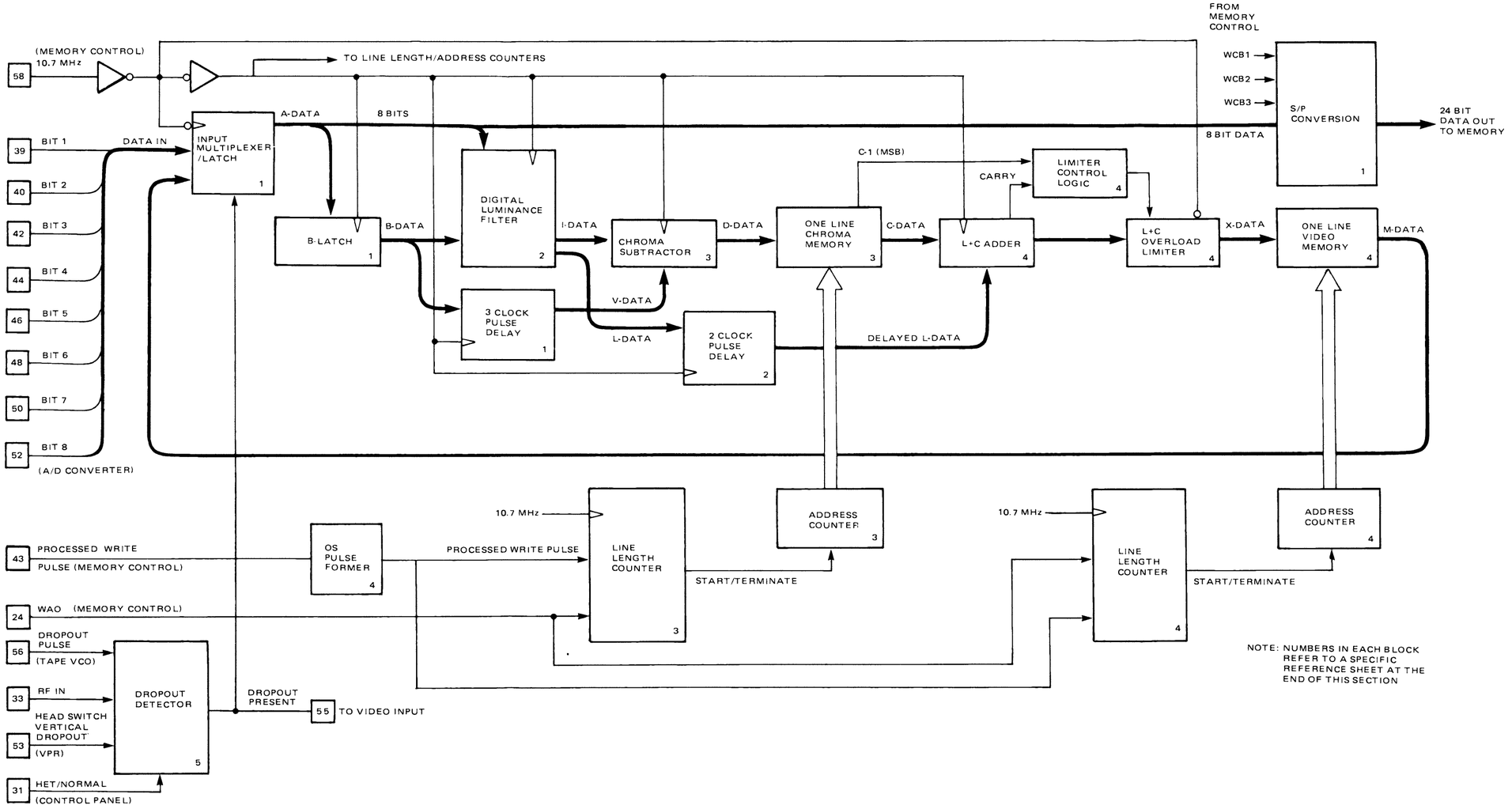


Figure 8-1.
Simplified Block Diagram

All operations are hard-wired. Divide-by-2 (U58, U67) is accomplished by a hard-wired shift right one bit. Divide-by-4 (U39, U48) is accomplished by a hard-wired shift right two bits. Divide-by-16 (U32, U22) is accomplished by a hard-wired shift right four bits.

For the purpose of analysis of the digital one-line dropout compensator, the chroma signal of the following example is considered to have the same phase as subcarrier (10.7 MHz clock). It is assumed that clocking occurs as indicated in Figure 8-1. The serial stream of 8-bit words from the A/D Converter PWA is latched into the input multiplexer by the 10.7 MHz clock. Sample A is the output of the B-latch. Sample B is the concurrent data on the A-bus. Sample C is the data on the A-bus on the following clock pulse. The three samples are shown in Figure 8-2.

The example in Figure 8-2 uses an arbitrary chroma positive peak value of 250, a chroma negative peak at 50, and a luminance value of 200. The average value of luminance is thus 150. Sampling occurs at +60 degrees, 0 degrees, and -60 degrees. (Sin 60 = 0.866) (0.866 X 100 = 87), or 87 bits. Therefore sample A = 150 + 87 = 237, sample B = 150, and sample C = 150 -87 = 63.

A + B = (236 + 150) = 386. 386 is an overflow condition. The sum at the output is 130 plus a carry-out of 1 (next highest bit). A hard-wired shift right is equivalent to a divide-by-two. Placing the carry in the MSB of the latch carries forward the 256-bit of the sum, downshifted to 128. The value 131 becomes 65.

$$\frac{A+B}{2} = 128 + 65 = 193$$

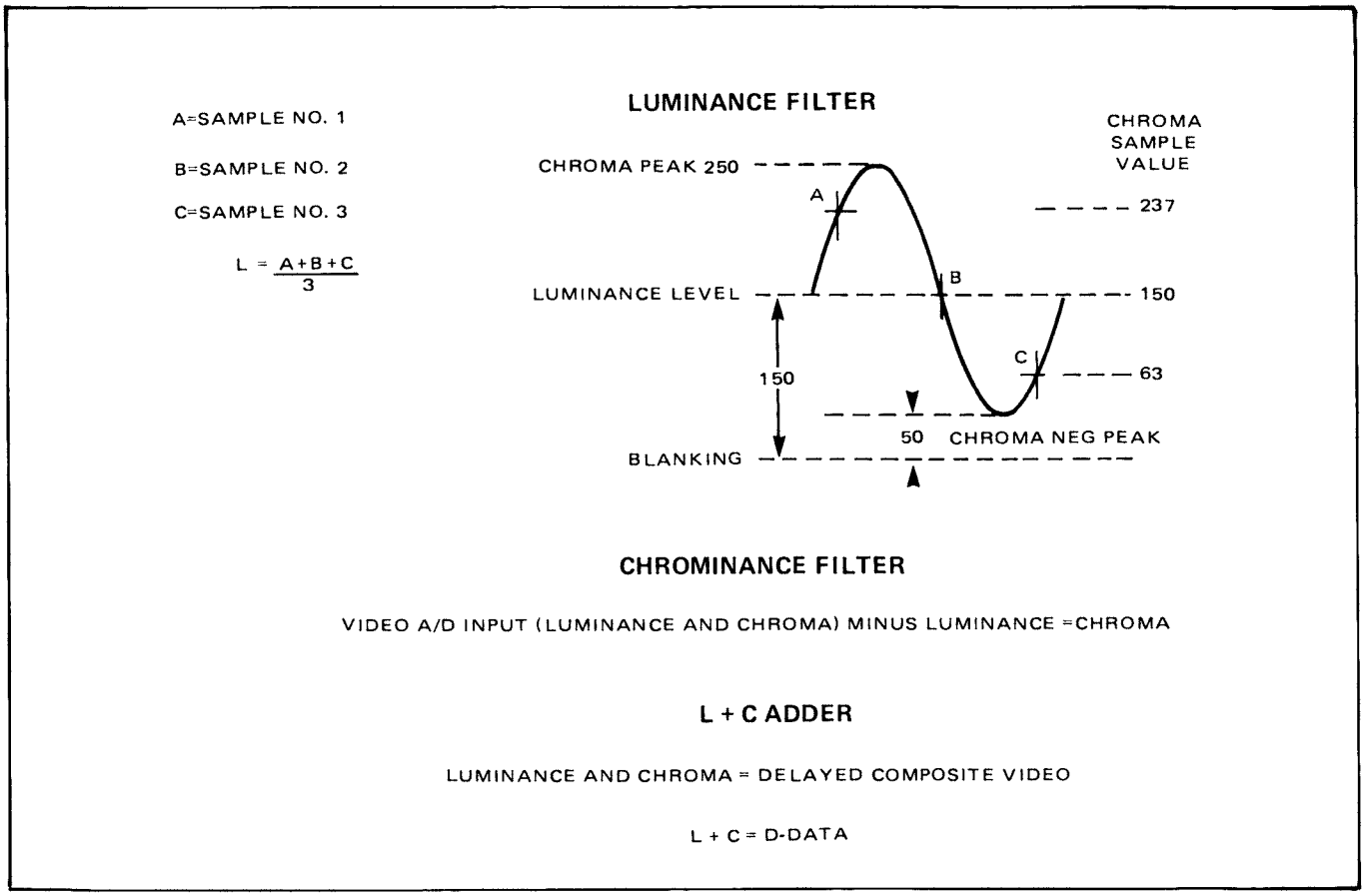


Figure 8-2. Digital One-Line Delay Equations

C/2 = 65/2 = 32. The C sample is hard-wired shift right one bit (divide-by-two)

$$\frac{A+B}{2}+\frac{C}{2}=(193+32)=225$$

The output of the second adder is hard-wired shift right one bit (divide-by-two). The carry out to the MSB of the latch is 0 in this example. Therefore, the latch output is 225/2 = 112 = S value

$$\frac{\frac{A+B}{2}+\frac{C}{2}}{2}=\frac{A+B+C}{4}=112=S$$

$$S/4+S=P=(112/4+112)=(28+112)=140$$

$$P/16+P=L=(140/16+140)=(8+140)=148=L$$

$$L=\frac{A+B+C}{3}=148$$

L-bar = 1's-complement-of-L = 256/148 = 108

8-5. Chrominance Subtractor. See REFERENCE 3. V-data is B-data delayed by three clock cycles to establish the comparison of luminance (average of three samples of video) with the value of the second sample of that group. V-data is applied to one set of inputs of the U30/21 adder. L-bar data is applied to the other input with a carry in of 1, making the L-bar data the 2's complement of L. Thus the operation is a binary subtraction. With luminance subtracted from luminance-and-chrominance (video) the result is chrominance.

8-6. Chroma Memory. See REFERENCE 3. Chroma is latched into the D-latch and forwarded to the chroma memory. When the write pulse starts the chroma address register the D-data is loaded into the memory and the previously stored line of data is read out to the C-latch.

L-data from the digital luminance filter is delayed by two clock cycles to match the processing delay of the chrominance subtractor. L-data and C-data are added to produce data representing the composite video signal. The result is routed to the L + C multiplexer/latch as shown in Figure 8-1.

In any group of three sequential samples, four clock pulses are required to derive the values of L and L-bar. Referring to Figure 8-3, at C' time the luminance value for samples A, B, and C is derived. The V-value which is added to L-bar in the chrominance adder is sample B. The next group of samples are labeled A', B', and C'. The luminance value for this group is derived at time C', and the sample to which it is added is sample B'. Thus a sequence of three sample groups, each advanced in time by one clock pulse, is compared with a continuous series of video samples to derive the values of chroma. Although three samples of video are required to produce a value for luminance, this value is valid only for one specific sample of video. The delayed video which is applied to the chroma adder is a first-in-first-out circuit; therefore, the video sample B is available at time C'.

8-7. Luminance Filter — Low-Pass Characteristic. The digital luminance filter is a band reject filter and exhibits some of the characteristics of an analog low-pass filter. At the boundary of a sharp transition in values (a gross change occurring between two samples of data) the summation of a group of three samples of video is distorted, and may result in a distortion of the processing chain. One example would be if the transition were from a "black" color bar to a saturated white color bar. Figure 8-3 illustrates the effect of the low frequency characteristic.

8-8. *L + C Overload Limiting. See REFERENCE 4.* If, as in color bars or split field color bars, a video signal of sharp transition and large change of scalar values is encountered, a high frequency transient is produced which could cause the transition to "ring" in the bandpass filter of the Video Output PWA.

A worst case example of the error condition and the correction applied by the error detection logic is a transition during a vertical split field. If chroma (2 lines past) and luminance (1 line past) cross the boundary of a color bar and a white bar, the chroma of the color bar and the luminance of the white bar would be added in the L + C adder. The addition of the two radically different video signals will result in an erroneous digital signal containing black spikes instead of the normal negative excursion of the chroma sine wave.

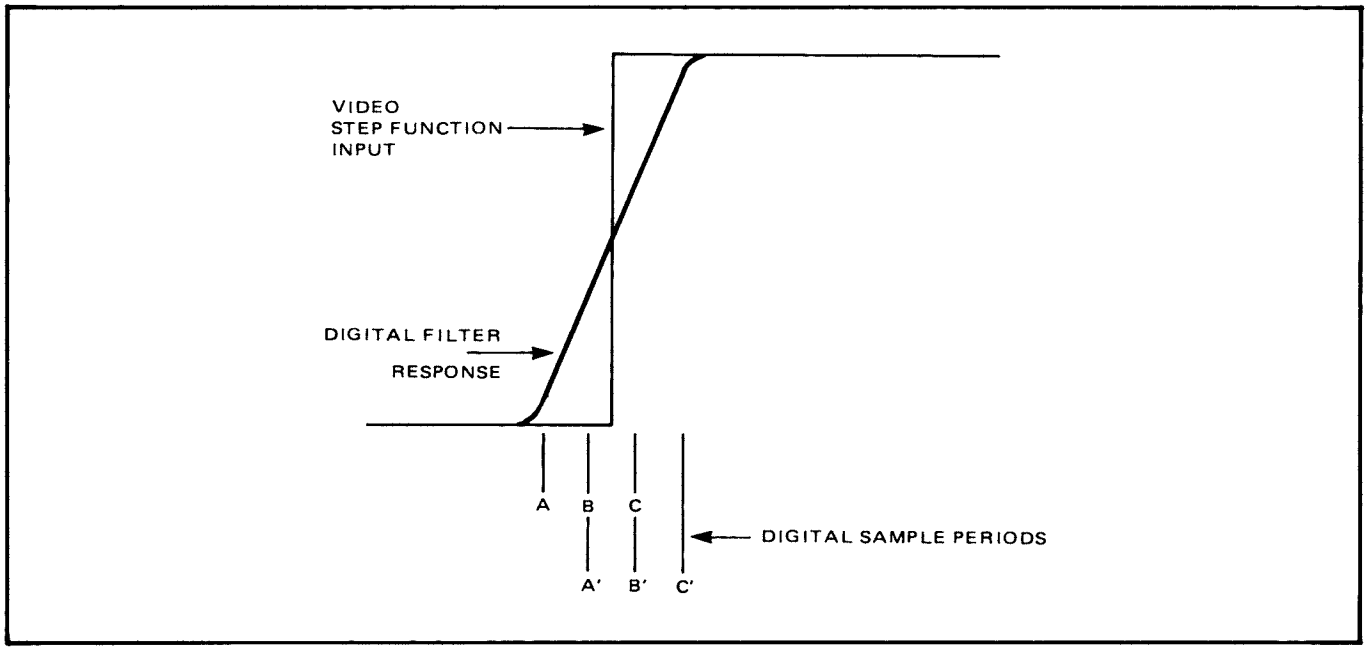


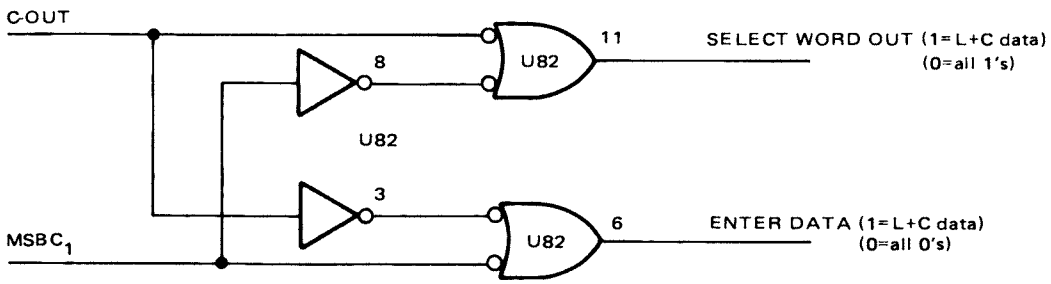
Figure 8-3. Digital Luminance Filter Sample Timing and Transient Response

The L + C multiplexer control logic will provide a limit of all 1's for the erroneous addition, and thereby prevent any unsuitable condition in the Video Output PWA. The L + C multiplexer logic and decodes are illustrated in Figure 8-4.

8-9. **Chroma and L + C Memories.** See REFERENCE 3 and 4. Nine clock cycles are required to process video data through the dropout compensator circuits. Without this compensation, a horizontal shift of video would occur when stored dropout data is substituted for off-tape video. To correct for this condition, data from the M-latch must be advanced by nine clock cycles toward the write pulse. In addition, the 1/2 cycle subcarrier shift on alternate lines must be reconciled to provide the DOC output M data with the previous line luminance plus chroma of two lines past. The memories and the memory address counters are the same for both the chroma and L + C memories, but the line length counters provide the data manipulation necessary for the delay and alternate line offset.

8-10. *Memory Organization and Address Counters.* One line of NTSC data (64 μs) would require 686 8-bit words. The picture video portion of the line, however, uses only 636 words. The chroma and L + C one-line memories use 256 X 4 bit RAM memory IC's organized as four 8 X 256-bit partitions. While one line of video needs only three partitions (768 words), the simultaneous write/read serial addressing scheme uses a fourth partition.

Compare the two memories with their address counters on REFERENCE 3 and 4. Note that the L + C memory address counter (U72, U63, U54, U44, and U43 on Reference Sheet 4) and the chroma memory address counters (U19 through U37 on REFERENCE 3) are exactly the same. Ignoring the line length start and terminate signals for the moment, it can be seen that as long as the 10.7-MHz clock is present the address counters continuously supply a sequence of addresses which advance the partition sequence counter (U36 for the chroma address counter) at the end of each 255 binary address count. The two-bit output of this counter is decoded as $\overline{OE1}$, $\overline{OE2}$, $\overline{OE3}$, and $\overline{OE4}$. The partition access code when applied to a write enable input (pin 20) on the RAM memories provides access to write into the memory in the addressed sequence; when applied to the read enable input (pin 18), it provides access to read data out to the 8-bit C-data latch. The write/read



INPUT CONDITION		OUTPUT CODE		MULTIPLEXER/LATCH OUTPUT
MSB	C-OUT	ENTER	SELECT	
1	1	1	1	L+C Data
1	0	0	1	All 0's Out (Error Condition)
0	1	1	0	All 1's Out (Error Condition)
0	0	1	1	L+C Data

Figure 8-4. Multiplexer Control

sequence shown in Tables 8-1 and 8-2 for the chroma and L + C memory partition addressing also illustrates how the fourth partition is used for the simultaneous write/read process. The line is read out of memory one partition behind the partition into which data is written.

Table 8-1. Chroma Memory Partition Sequence

WRITE ENABLE	PARTITION	READ ENABLE	PARTITION
$\overline{OE1}$	U2/U1	$\overline{OE1}$	U27/U26
$\overline{OE2}$	U27/U26	$\overline{OE2}$	U18/U17
$\overline{OE3}$	U18/U17	$\overline{OE3}$	U10/U9
$\overline{OE4}$	U10/U9	$\overline{OE4}$	U2/U1

Table 8-2. L + C Memory Partition Sequence

WRITE ENABLE	PARTITION	READ ENABLE	PARTITION
$\overline{WE1}$	U80/U79	$\overline{WE1}$	U71/U70
$\overline{WE2}$	U71/U70	$\overline{WE2}$	U62/U61
$\overline{WE3}$	U62/U61	$\overline{WE3}$	U53/U52
$\overline{WE4}$	U53/U52	$\overline{WE4}$	U80/U79

The picture video line requires only 636 words of the possible 768 words of three partitions. By loading the address counters with a binary 44, each partition advance occurs after 212 address counts. This maintains the write/read partition sequencing but it should be noted in the case of the L + C line length counter that the start of the video line data need not occur with the first

memory address (binary 44). The line length counters control the start and termination of the address counter clocks, and the start of the consecutive partition address of the video line in memory may position the data anywhere in the memory.

8-11. *Chroma Line Length Counter.* See REFERENCE 3. The chroma line length counter uses the carry from the two stages of the address counter to advance another counter (U11) three counts. This produces a line length of 212 counts times three, or 636 clock cycles. At startup the line length carry from U11 will be clocked through the terminate flip-flop U4, to inhibit the address counter clock. This will bring the line count in sync with the address count when the processed write pulse enables the next line. Thus, the chroma line data will always reside in memory across any three partitions with the start of the line always at binary address 44.

The M data consists of chroma from 2 lines previous and luminance from the previous line. The chroma line length counter is used to manipulate the data to reconcile the subcarrier phase displacement relative to the start of the line initiated by the processed write pulse from the Memory Control PWA. On alternate lines, WA0 (7.8 kHz) is used to pre-load counter U12 to a 12 or 13 count. The address counter clock from U5-8 is thus inhibited for the 3 or 2 clock cycle period needed to lock the U12 carry output high. This re-times the chroma processing to make the previous line chroma phase consistent with the current line luminance.

8-12. *L + C Memory Line Length Counter.* See REFERENCE 4. The L + C line length counter is used to advance the M data read toward the processed write pulse to compensate for the nine cycle delay through the dropout compensator processing. Also, the output M data must be consistent in chroma phase relative to the write pulse on alternate lines to reproduce the 1/2 cycle subcarrier shift.

The processed write pulse from U6-5 initiates the L + C line counter (U59, U68, U78, and U85). The line counter operates independently of the address counter and the start/terminate output at U85-9 merely inhibits or enables the address counter clock. Thus the start of the data line is not coincident with any particular memory address and will advance across partition boundaries as the line length counter manipulates the data. The address counter of the L + C memory stops at the termination of the line length counter, but *is not reset.* At the start of the following line the address count is continued until the line terminates again. By this means, the last address of the L + C "line" is advanced nine words past the number of words stored in the memory, and data read out is advanced by nine clock cycles. Thus data from the M-latch is matched to A/D input data in reference to the write pulse, and there is no horizontal offset of substitute data during a dropout condition.

Note that the line length counter is loaded to binary 3451 by the processed write pulse start. At the final carry from U78 at binary 4096 the counter will have been counting a total of 645 clock periods. This means that the address counter has produced the normal line 636 addresses plus nine. The address counter of the L + C memory stops at the termination of the line length counter, but *is not reset.* At the start of the following line the address count is continued until the line terminates again. By this means, the last address of the L + C "line" is advanced nine words past the number of words stored in the memory, and data read out is advanced by nine clock cycles. Thus data from the M-latch is matched to A/D input data in reference to the write pulse, and there is no horizontal offset of substitute data during a dropout condition.

In the main TBC memory the hue of the video data does not shift because the phase of chroma relative to burst is entered into memory intact. However, the 1/2 cycle of subcarrier phase shift per line must be accounted for in the manipulation of the processed dropout data to avoid a sawtooth effect at the edge of the screen during multi-line dropouts. To accommodate the alternate line subcarrier phase shift the line length counter pre-load is shifted from 3451 to 3453 by the 7.8 kHz WA0 signal. This advances the L + C line by two clock cycles, so that as the L + C data is read out the subcarrier shift and the processor delay both will be reconciled.

8-13. Dropout Detector Circuit. See REFERENCE 5. The dropout detector circuit receives information from three sources: (1) gated dropout pulse from the Tape VCO PWA (2) rf in from a heterodyne VTR (3) head switch dropout from the VPR which inhibits dropout operating during the vertical interval. The HET/NORMAL signal from the mode switch inhibits the gated dropout pulse signal and enables the rf detector in heterodyne mode. It also inhibits the head switch dropout gate in heterodyne mode. When the mode switch is in the normal position the reverse of these conditions is true.

The pulse stretcher extends the dropout signal for the input multiplexer by an additional 10 microseconds after the end of a dropout detection. The quality of the off-tape video is not fully restored immediately after the end of the dropout. The stretched pulse is, therefore, required to extend to the replacement period.

8-14. DESCRIPTION – SERIAL-TO-PARALLEL CONVERTER (1409122)

See the block diagram on REFERENCE 8.

8-15. Functional Description

The function of this assembly is to accept a serial train of 8-bit words at 3-Fsc rate (10.7 MHz), from the Analog-to-Digital Converter PWA 4 and store them in a 24-bit output latch from which they are written into the Memory PWA's 9, 10, and 11 at Fsc rate (3.58 MHz).

8-16. Serial-to-Parallel Conversion. The 8-bit words are clocked into the 24-bit input latch by the clock signals from the Memory Control PWA 7. The order of loading is WCB1 bits 1 to 8, WCB2 bits 9 to 16, WCB3 bits 17 to 24. At the following WCB1 time, the complete 24-bit word is clocked into the output latch. Clock signals WØ1 and WØ2 at WCB1 time but slightly delayed in phase, clock the data into memory. The write clock sequence for each line of video data is initiated by the write pulse from the Tape H Comparator PWA 5.

8-17. S/P CONVERTER (ONE-LINE DROPOUT COMPENSATOR) (1409140) MAINTENANCE

See REFERENCE 7 in this section for the component locator diagram, jumper/test point/adjustable components summaries, and the waveforms called out in these procedures.

Before undertaking any adjustments to the S/P Converter review the *System Alignment Guide* (Table 3-2) and the *Tape/Reference Test Loop* discussion (paragraph 3-5) in the *System Maintenance* section (Part I) for a general understanding of the scope of these field adjustments.

Consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the S/P Converter PWA and interactive functions between it and other PWA's before making any adjustments.

8-18. Dropout Test (VTR's with TTL Dropout Pulse)

This test requires a dropout test tape from those listed in Table 3-2, *Test Equipment and Tools,* in the *System Maintenance* section (Part I).

1. Verify operation of the dropout compensation option in normal speed playback.

   a. Switch the DOC option off with the DOC ON/OFF switch on the front edge of the S/P Converter PWA 8.

   b. Play back the special dropout tape. A dropout will appear in the picture.

   c. Switch the DOC on (DOC ON/OFF PWA 8). The dropout noted in step 1b should be removed.

   NOTE

   Some marks around the dropout area may show – this is normal.

2. Play back tape in STILL FRAME and SLOW MOTION. Repeat observations of step 1c.

NOTE

Special dropout tapes are intended *only for use in the procedure given above. Use of this tape for other purposes is not recommended.*

8-19. RF Dropout Level Adjustment

The rf dropout detector is used for the Ampex VPR-20, heterodyne, and other VTR's which do not supply a TTL dropout pulse. The rf dropout detector is calibrated at the factory for optimum dropout recovery and only the level may need adjustment for particular VTR's. More elaborate adjustment of the detector circuit for purposes of repair is given in the next paragraph. This procedure uses the programmed dropout test tape listed in *Test Equipment and Tools,* Table 3-1, in the *System Maintenance* section.

1. Verify that jumper J2 is in B–C position.
2. Switch dropout compensator (DOC) off (S1, PWA edge).
3. Play dropout tape at normal speed and observe two small dropouts near the top and bottom of the picture and a large dropout in the center.
4. Switch DOC on. Dropouts observed above should be removed.
5. If dropouts are not removed or other picture disturbance indicates an incorrect dropout level, adjust R24 (RF D.O. level – PWA edge) for a stable picture.

NOTE

If a dropout test tape is not available, a 20-dB pad inserted in the line to the RF IN jack may be used to simulate a typical dropout level. Adjust R24 during normal playback of color bars for disturbance in the picture with pad installed, then remove pad and verify a normal picture.

8-20. RF Dropout Detector Adjustment

This procedure may be used in lieu of a programmed dropout test tape.

NOTE

Because of noise and crosstalk with the PWA on the extender, adjustment results here should be rechecked with the PWA in the card rack.

1. RF threshold and amplifier gain adjustment:

   a. Verify that jumper J2 is in the B–C position (rf dropout enable).

   b. Connect oscilloscope –

   Channel 1: PWA 3 – TP1 (Tape video input)

   Channel 2: U7-7 (RF comparator output)

   Trigger: Internal

   c. Disconnect TAPE VIDEO IN on back panel to remove the rf source.

   d. With video input disconnected, adjust R24 (AGC level) for a transition from low to high. Signal should remain high. Signal at TP5 should be less than the dc voltage at the junction of R13 and R4 (threshold level).

   e. Connect oscilloscope –

   Channel 1: PWA 3 – TP5 (Tape video input)

   Channel 2: PWA 8 – TP5 (RF amplifier output)

   Trigger: PWA 8 pin 24 (WA0)

   f. Connect a tape video source to TAPE VIDEO IN connector.

g. Adjust oscilloscope time base to view horizontal sync time period. (RF is lowest in frequency at this period.)

h. Adjust R44 for 500 mV of rf at TP5. The signal is very noisy. See waveform 56 (S).

i. Connect oscilloscope —

Channel 1: PWA 3 — TP1 (Tape video Input)

Channel 2: PWA 8 — U24-12 (RF detector one-shot)

Trigger: PWA 8 pin 24 (WA0)

j. With video input connected, view horizontal sync time period. Adjust R25 until pulses appear. Readjust until pulses disappear and signal on U24-12 is a continuous low. The objective is to make timeout of the retriggerable one-shot slightly longer than the period of 1 Hz of the lowest frequency of rf.

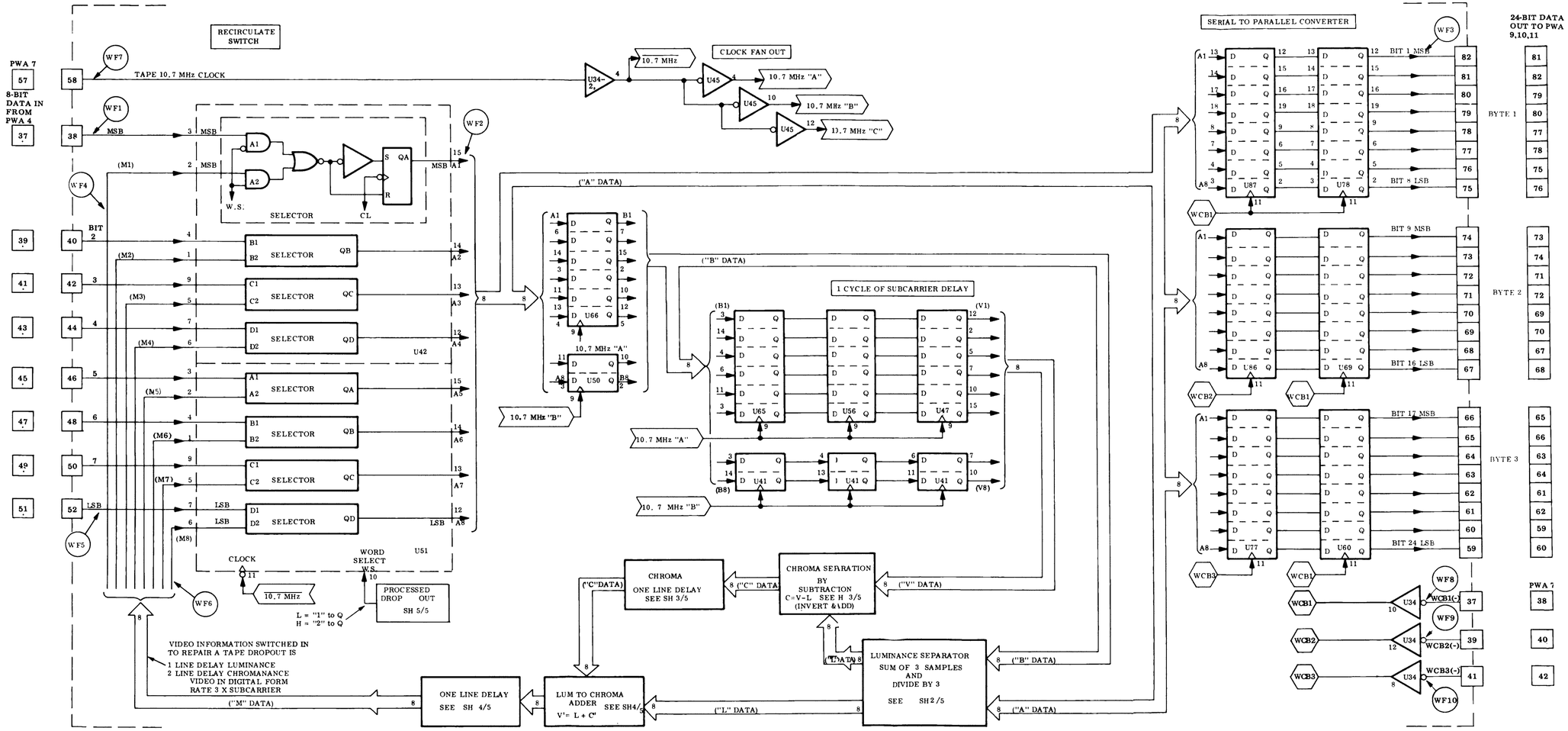
2. Pulse stretcher adjustment:

a. Connect oscilloscope —

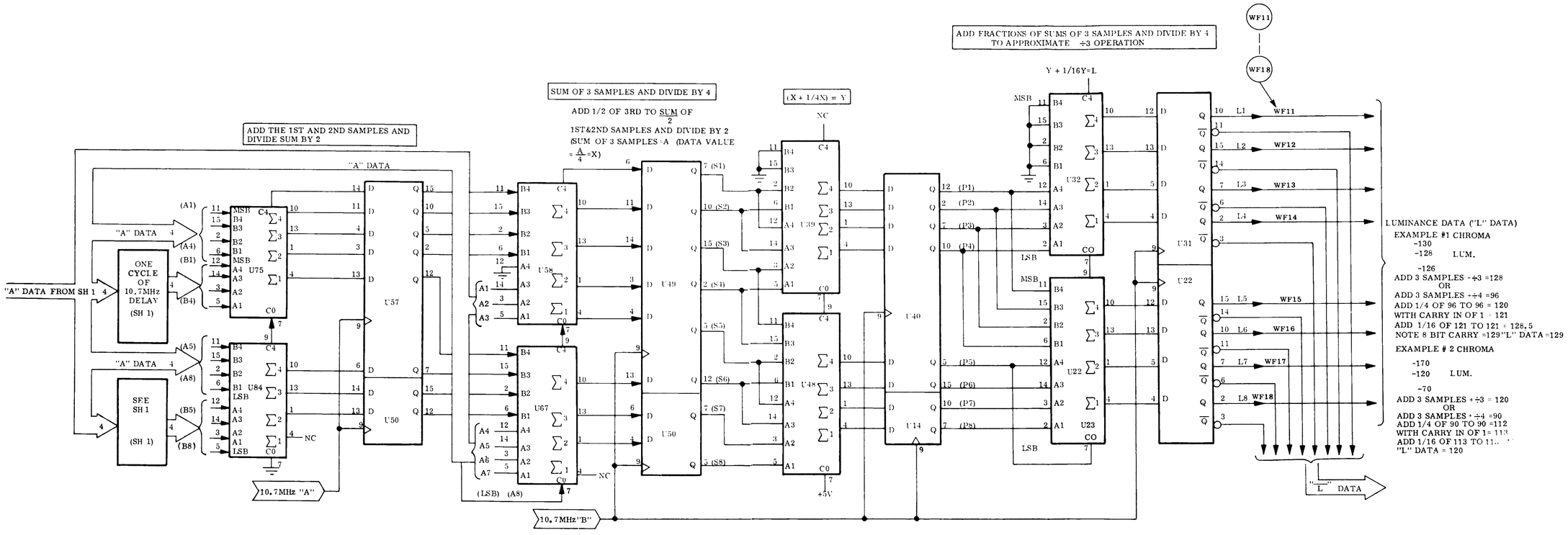
Channel A: (pulse stretcher one-shot)

Trigger: PWA pin 24 (WA0)

b. Adjust R29 (pulse stretcher adjustment) for a negative-going pulse of 9.0 to 9.2 microseconds.

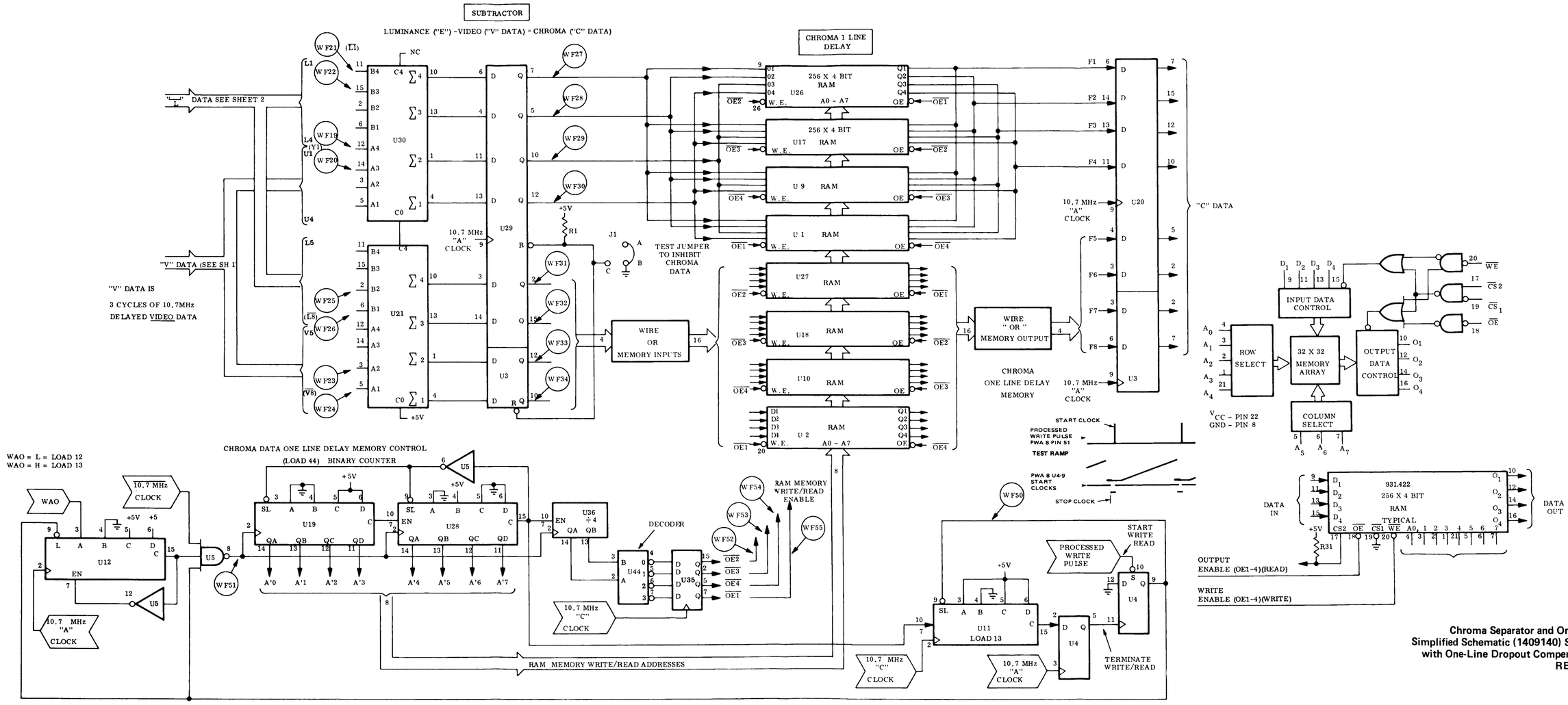


Overall Detailed Block Diagram (1409140)
S/P Converter with One-Line
Dropout Compensator PWA 8
REFERENCE 1

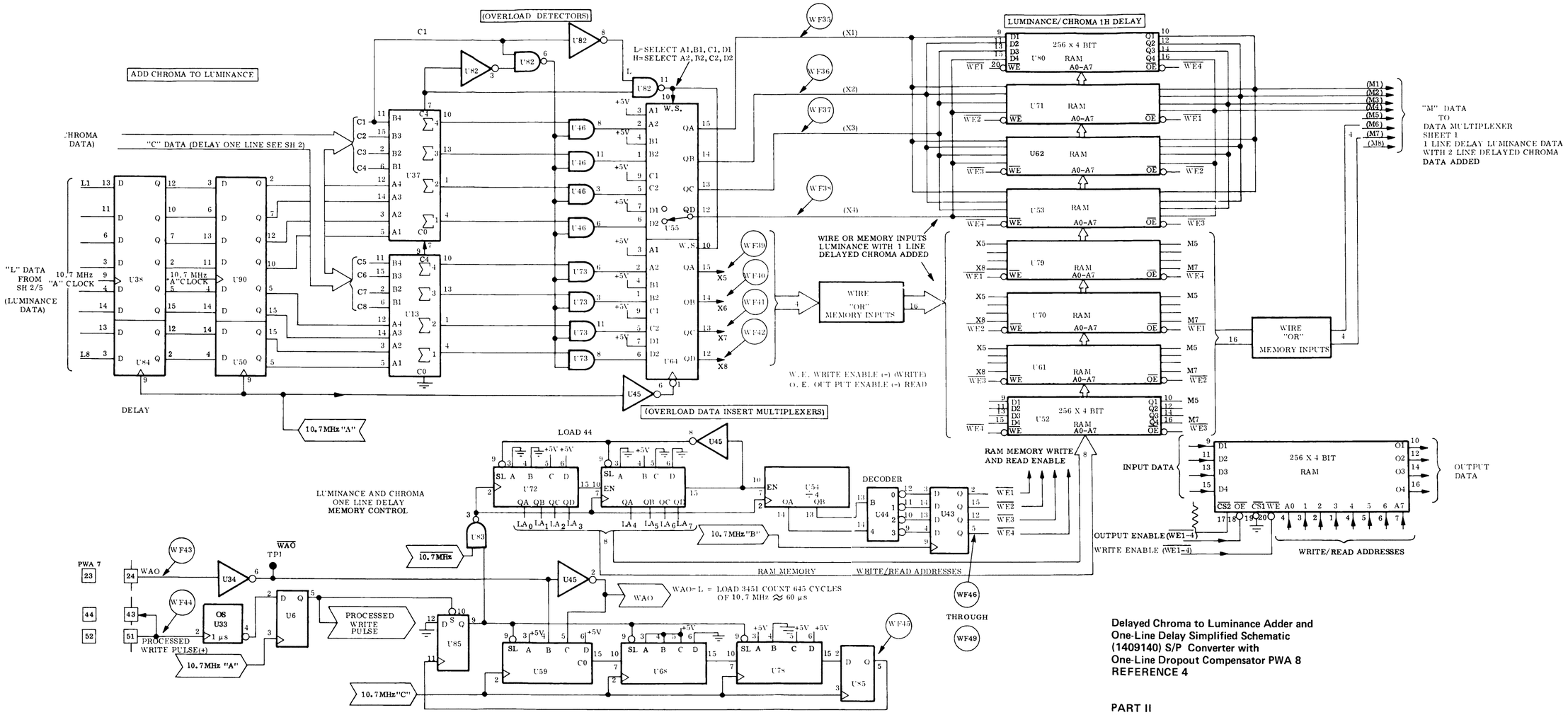


Luminance Filter Simplified Schematic
(1409140) S/P Converter with
One-Line Dropout PWA 8
REFERENCE 2

AMPEX 1809474-01

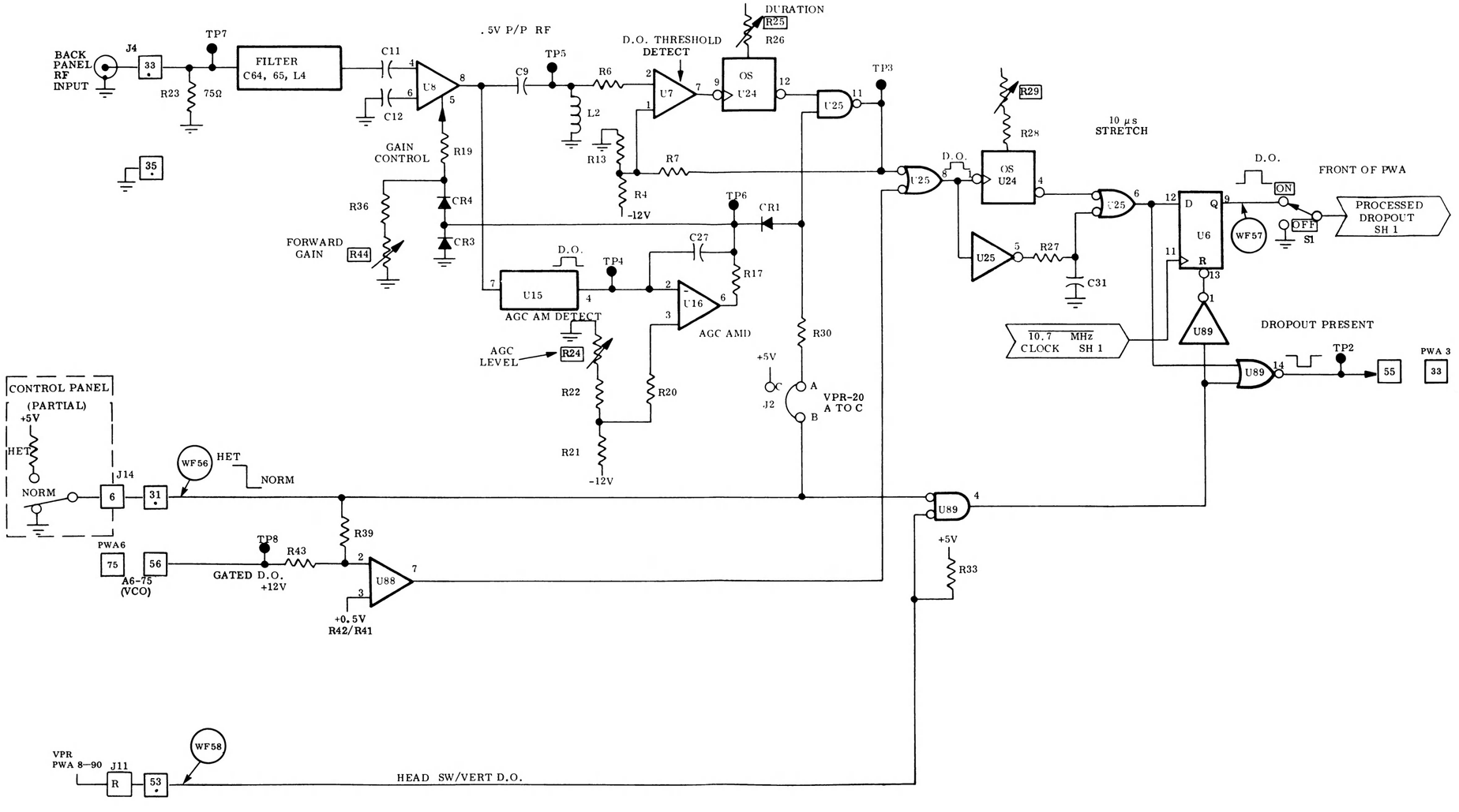


Chroma Separator and One-Line Delay Simplified Schematic (1409140) S/P Converter with One-Line Dropout Compensator PWA 8 REFERENCE 3



Delayed Chroma to Luminance Adder and One-Line Delay Simplified Schematic (1409140) S/P Converter with One-Line Dropout Compensator PWA 8 REFERENCE 4

AMPEX 1809474-01



INSERT TEST RAMP (PWA 3 J4 B–C) — **A**

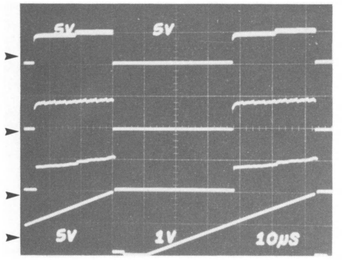
PIN 38 BIT 1 MSB — WF1

U42-15 RECIRCULATE OUTPUT ("A" DATA) — WF2

PIN 82 — WF3

PWA 4 TP4 (TEST RAMP)

TRIG: PIN 24



INSERT TEST RAMP (PWA 3 J4 B–C) — **B**

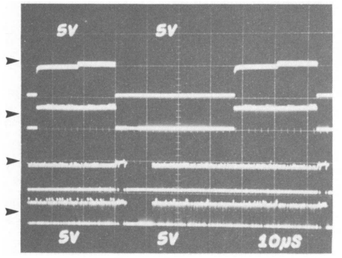
PIN 38 BIT 1 MSB — WF1

U42-2 PROCESSED "M" DATA MSB — WF4

PIN 52 BIT 8 LSB — WF5

U51-6 "M" DATA LSB — WF6

TRIG: PIN 24



C

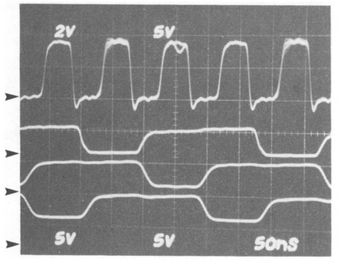
PIN 58 TAPE 10.7-MHz CLOCK — WF7

PIN 37 WCB1 — WF8

PIN 39 WCB2 — WF9

PIN 41 WCB3 — WF10

TRIG: PIN 41



RF Dropout Detection Simplified Schematic
(1409140) S/P Converter with One-Line
Dropout Compensator PWA 8
REFERENCE 5

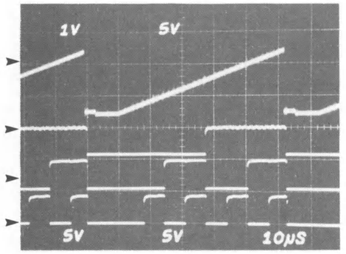
INSERT TEST RAMP (PWA 3 J4 B-C)

D

PWA 4 TP4 TEST RAMP

"L" DATA
- U31-10 L1 — WF11
- U31-15 L2 — WF12
- U31-7 L3 — WF13

TRIG: PIN 24

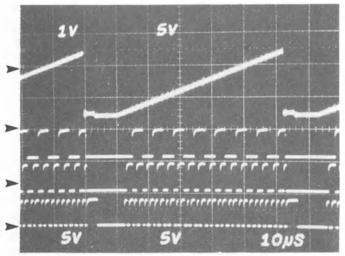


E

PWA 4 TP4 TEST RAMP

"L" DATA
- U31-3 L4 — WF14
- U22-15 L5 — WF15
- U22-10 L6 — WF16

TRIG: PIN 24

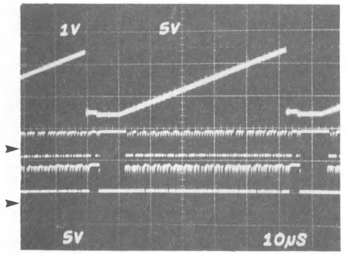


F

PWA 4 TP4 TEST RAMP

"L" DATA
- U22-7 L7 — WF17
- U22-2 L8 — WF18

TRIG: PIN 24

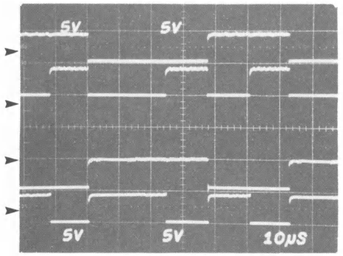


TEST RAMP **G**

"V" DATA
- U30-12 V1 — WF19
- U30-14 V2 — WF20

"$\overline{L}$" DATA
- U30-11 $\overline{L1}$ — WF21
- U30-15 $\overline{L2}$ — WF22

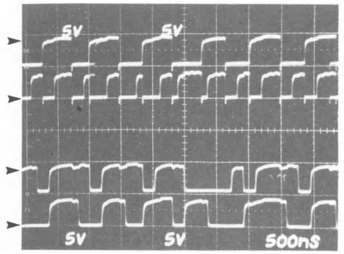
TRIG: PIN 24



TEST RAMP **H**

- U21-3 V7 — WF23
- U21-5 V8 — WF24
- U21-2 L7 — WF25
- U21-6 L8 — WF26

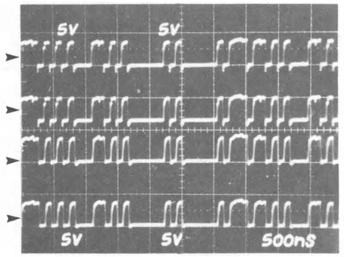
TRIG: PIN 24
TEST RAMP INSERTED A3J4



TEST RAMP **I**

L-V SUB-TRACTOR OUTPUT
- U29-7 MSB — WF27
- U29-5 — WF28
- U29-5 — WF29
- U29-12 — WF30

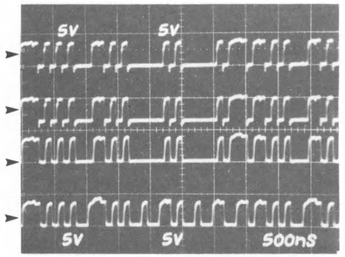
TRIG: PIN 24



TEST RAMP **J**

L-V SUB-TRACTOR OUTPUT
- U29-2 — WF31
- U29-15 — WF32
- U3-12 — WF33
- LSB U3-10 — WF34

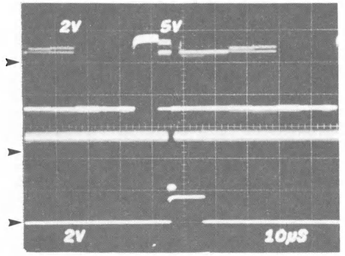
TRIG: PIN 24



K

- PIN 38 BIT 1 MSB — WF1
- PIN 56 (TP8) GATED DROPOUT — WF56
- U6-9 (S1) PROCESSED DROPOUT — WF57

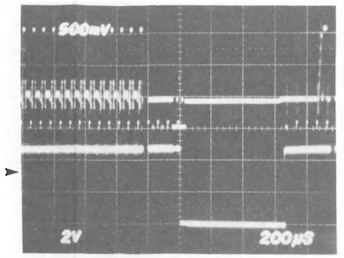
TRIG: PIN 53
VPR IN STILL MODE SCANNING A DROPOUT



VIDEO TO A/D CONVERTER PWA 4 TP4 **L**

- PIN 53 VPR HEAD SWITCH V DROPOUT — WF58

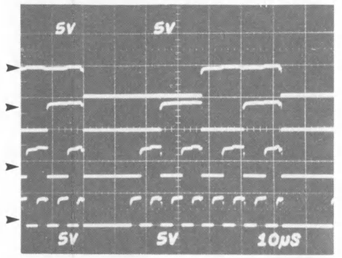
TRIG: PIN 53
VPR IN NORMAL PLAY



TEST RAMP **M**

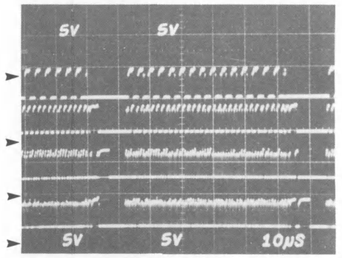
L+C DATA
- U55-15 BIT 1 — WF35
- U55-14 BIT 2 — WF36
- U55-13 BIT 3 — WF37
- U55-12 BIT 4 — WF38

TRIG: PIN 24



N

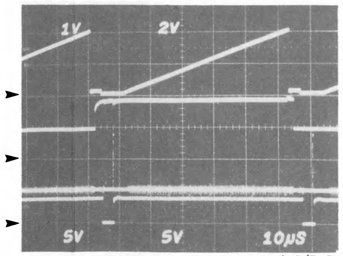
L+C DATA
- U64-15 BIT 5 — WF39
- U64-14 BIT 6 — WF40
- U64-13 BIT 7 — WF41
- U64-12 BIT 8 — WF42



TEST RAMP **O**

- PIN 24 WAO — WF43
- PIN 51 PROCESSED WRITE PULSE — WF44
- U85-9 ONE-LINE DELAY WRITE — WF45

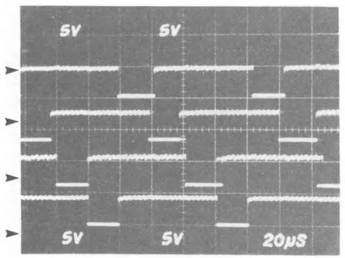
TRIG: PIN 24



TEST RAMP **P**

- U43-2 WE1 — WF46
- U43-15 WE2 — WF47
- U43-12 WE3 — WF48
- U43-5 WE4 — WF49

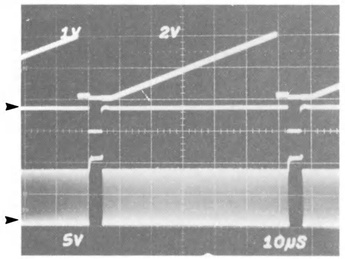
TRIG: U43-2



TEST RAMP **Q**

- U4-9 START CLOCKS — WF50
- U5-8 CHROMA DELAY CLOCK — WF51

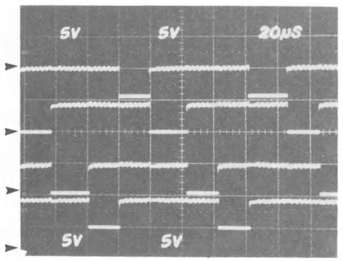
TRIG: PIN 24



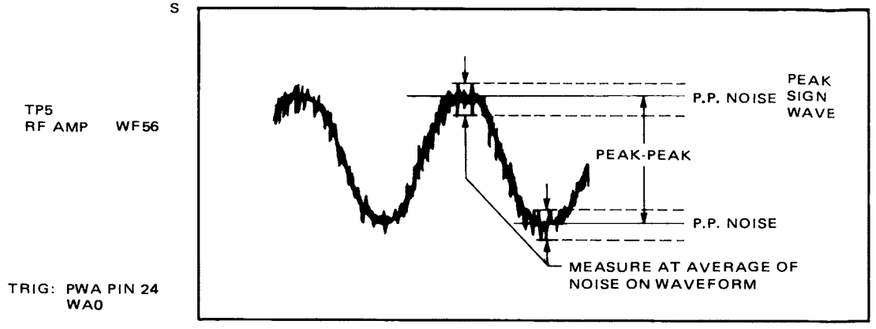
TEST RAMP **R**

- U35-15 OE2 (OUTPUT ENABLE) — WF52
- U35-2 OE3 — WF53
- U35-5 OE4 — WF54
- U35-7 OE1 — WF55

TRIG: U35-15

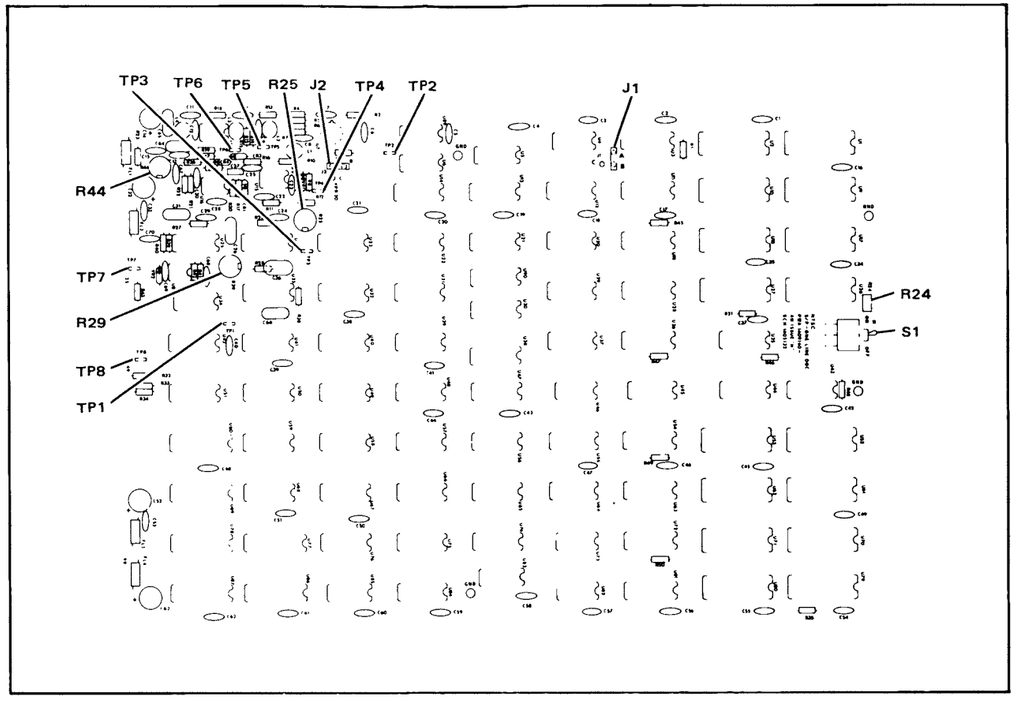


Waveforms (1409140) S/P Converter
with One-Line Dropout Compensator PWA 8
REFERENCE 6



PWA 8 Test Points

TEST POINT	NAME
TP1	Write address zero ($\overline{WA0}$)
TP2	Dropout present
TP3	Duration
TP4	Discriminator output
TP5	Gain controlled amplifier output
TP6	AGC amplifier output
TP7	RF input
TP8	TTL dropout pulse



PWA 8 Component Locator

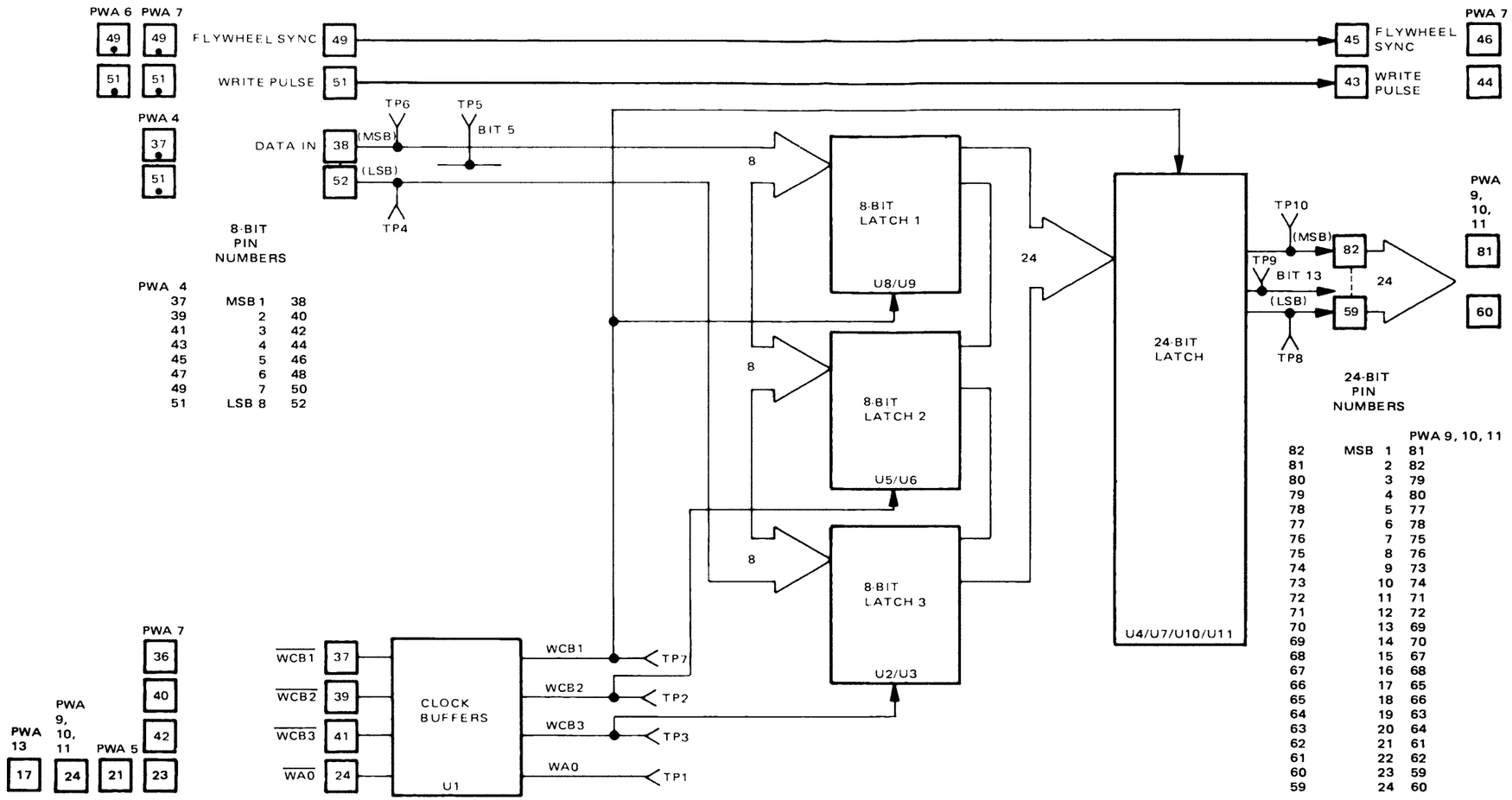
PWA 8 Adjustable Components

COMPONENT	FUNCTION
R24	AGC level
R25	Duration
R44	Forward gain
R29	Dropout pulse stretcher
S1	D.O.C. on/off

PWA 8 Jumpers

JUMPER	POSITION – FUNCTION	
J1	A–B	Normal
	B–C	Data disable
J2	A–B	RF dropout enable (VPR)
	B–C	TTL dropout enable

Test Points, Adjustable Components, Component Locator Jumpers (1409140) S/P Converter with One-Line Dropout Compensator PWA 8 REFERENCE 7



PWA 8 (1409122) Test Points

TEST POINT	NAME
TP1	Write address zero
TP2	Write clock byte 2
TP3	Write clock byte 3
TP4	LSB
TP5	5th MSB
TP6	MSB
TP7	Write clock byte 1
TP8	LSB byte 3
TP9	5th MSB byte 2
TP10	MSB byte 1
TP11	Ground
TP12	Ground
TP13	+5V

NOTE:

REFER TO WAVEFORMS A, B, AND C ON REFERENCE SHEET 11 FOR TYPICAL CLOCK AND LATCH SIGNALS.

Test Points Block Diagram (1409122)
S/P Converter (No D.O.C.) PWA 8
REFERENCE 8

SECTION 9 (10, 11)

MEMORY

DESCRIPTION AND MAINTENANCE

9-1. INTRODUCTION

Refer to the following documents in the *Parts Lists and Schematics* manual:

ASSEMBLY No. 1409107

SCHEMATIC No. 1402383

Numbered data sheets (REFERENCE 1, 2, 3 . . . *n*) to which PWA descriptions and maintenance procedures refer are located at the end of this section as follows:

Detailed Block Diagram – REFERENCE 1

Waveforms – REFERENCE 2

Maintenance Data – REFERENCE 2

MEMORY PWA 9
FUNCTION SUMMARY:

- Memory stores 12 H-lines of 24-bit data. PWA 9 stores lines 1–4; PWA 10 stores lines 5–8; PWA 11 stores lines 9–12. Write timing is synchronous to tape timing; read timing synchronous to reference video.

9-2. DESCRIPTION

Memory PWA's 9, 10, and 11 are a 12-line storage mechanism for quantized digital video signal from Serial-to-Parallel Converter PWA 8. Control of data in and data out of memory is under the direction of Memory Control PWA 7. Time-base correction of the digital data is accomplished by storing and accessing 24-bit data words in the Memory PWA's under control of separate read and write timing and addressing signals from the Memory Control PWA. Each Memory PWA is identical and each provides storage for four horizontal lines.

Three 8-bit words in a 24-bit parallel data format are presented to the inputs of the memories. The 24-bit words are clocked into a given line of memory at Fsc rate by a two-phase clock synchronized with tape-derived Fsc signal from the Memory Control PWA. At a later time they are clocked out of memory at an Fsc rate which is slaved to the station master sync generator. It is this process which accomplishes the primary time-base correction of errors due to error recorded on the tape or operation of the playback mechanism.

9-3. Memory Shift Registers

Each line of memory is made up of six 1024-bit dynamic shift registers. Each register is organized as four 256-bit shift registers. Each 256-bit register is further configured as two parallel registers, with $\phi 1$ clock entering the first bit of data into one of the parallel registers, and $\phi 2$ clock entering the second bit of data into the other parallel register. The third bit is entered into the first of the parallel registers by the next $\phi 1$ clock, the fourth bit of data into the second parallel register by the following $\phi 2$ clock, etc., until all 256 bits have been shifted. In the read cycle the data will be shifted out in the same order, first-in, first-out. (See Figure 9-1, *Shift Register* Block Diagram.)

9-4. Memory Organization

The 24-bit data words are presented to all 12 lines of memory in parallel. However, only the line currently addressed by the Memory Control PWA will have its write gates enabled. Memory logic decodes WMA–WA0–WA1 as line 1 address on PWA 9. (See block diagram in REFERENCE 1.)

The next event in the WMA–WA0–WA1 sequence will be decoded as line 2. The next as line 3, then line 4. In the following sequence WMB–WA0–WA1 will sequentially address lines 5, 6, 7, and 8 on

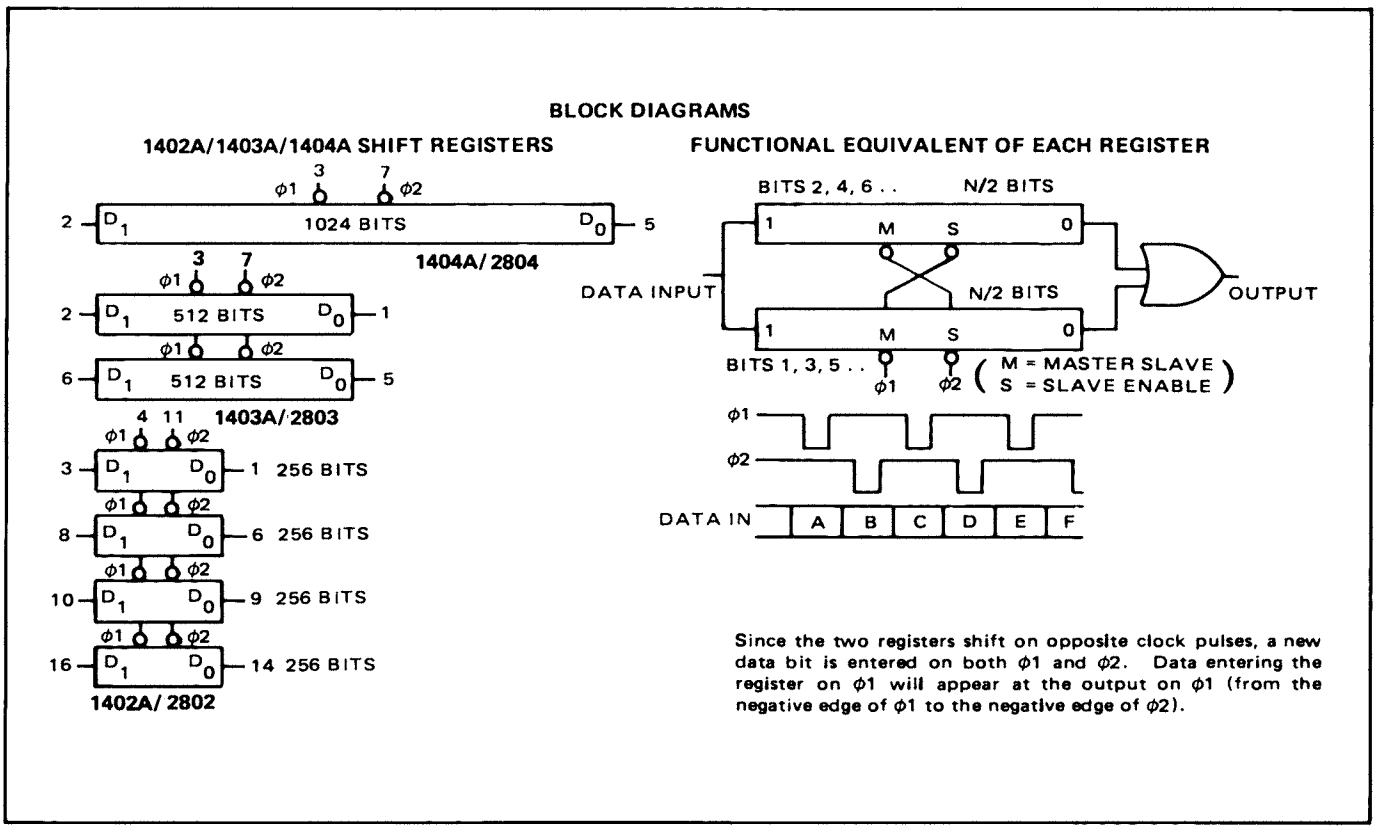


Figure 9-1. Shift Register Block Diagram

PWA 11. WMC–WA0–WA1 will address lines 9, 10, 11, and 12 in similar fashion.

The read decode logic will access line 1 of PWA 9 with RMA–RA0–RA1. In a manner similar to the write address it will access lines 2, 3, and 4 in sequence. RMB–RA0–RA1 will sequentially access lines 5, 6, 7 and 8 on PWA 11, and lines 9, 10, 11 and 12 will be accessed by RMC–RA0–RA1.

With a six-line difference in location, as data is written into memory, previously written data is simultaneously read out of memory; i.e., as line 6 is written, line 1 is read, then line 7 is written while line 2 is read, etc., until line 12 is written while line 7 is read. Then line 1 is written as line 8 is read and so on. The Memory Control PWA maintains the six-line difference in the read/write relationship to avoid a coincident read-write operation on a line. Although the shift register could clock data in and out of the register simultaneously using the same clock, the TBC, even in normal play, does not operate the read clock and the write clock with exact coincidence; therefore a simultaneous read-write on a line would thoroughly scramble the data.

All the most-significant bit outputs of the shift registers are wire-OR'ed together on a given Memory PWA to a bit 1 driver gate. Bit 2 is similarly wire-OR'ed to a bit 2 driver gate, and so on to bit 24. Outputs of the bit 1 driver gates of PWA 10 and 11 are wire-OR'ed by the motherboard. Bit 2 driver gates of PWA 9, 10, and 11 are similarly wire-OR'ed, and so on to bit 24. (See Figure 9-2, *Memory Organization* Simplified Block Diagram.)

9-5. Dual Load

Of the 12 lines of memory, the read function for a given read timing decode (i.e., RMA line 1)

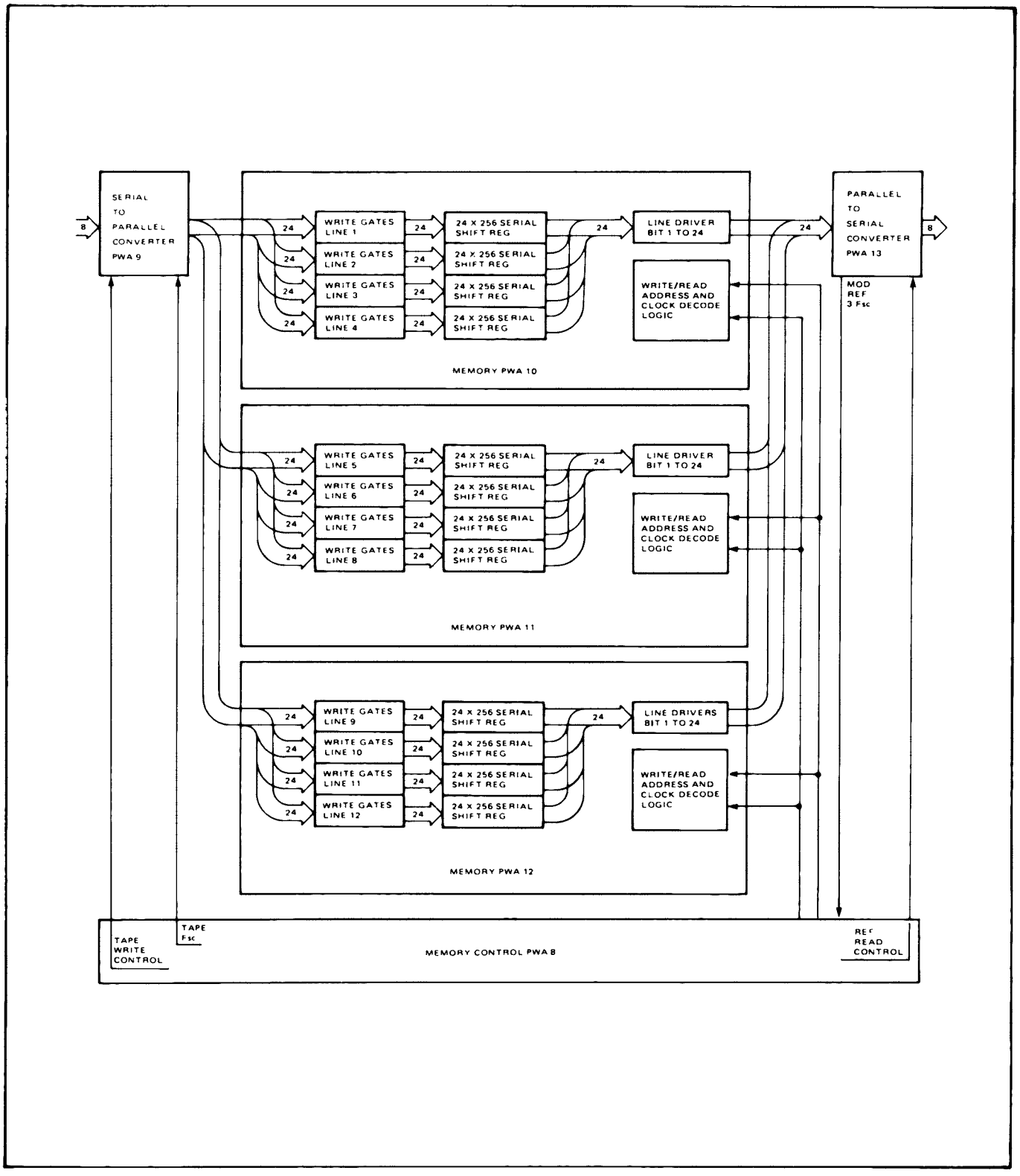
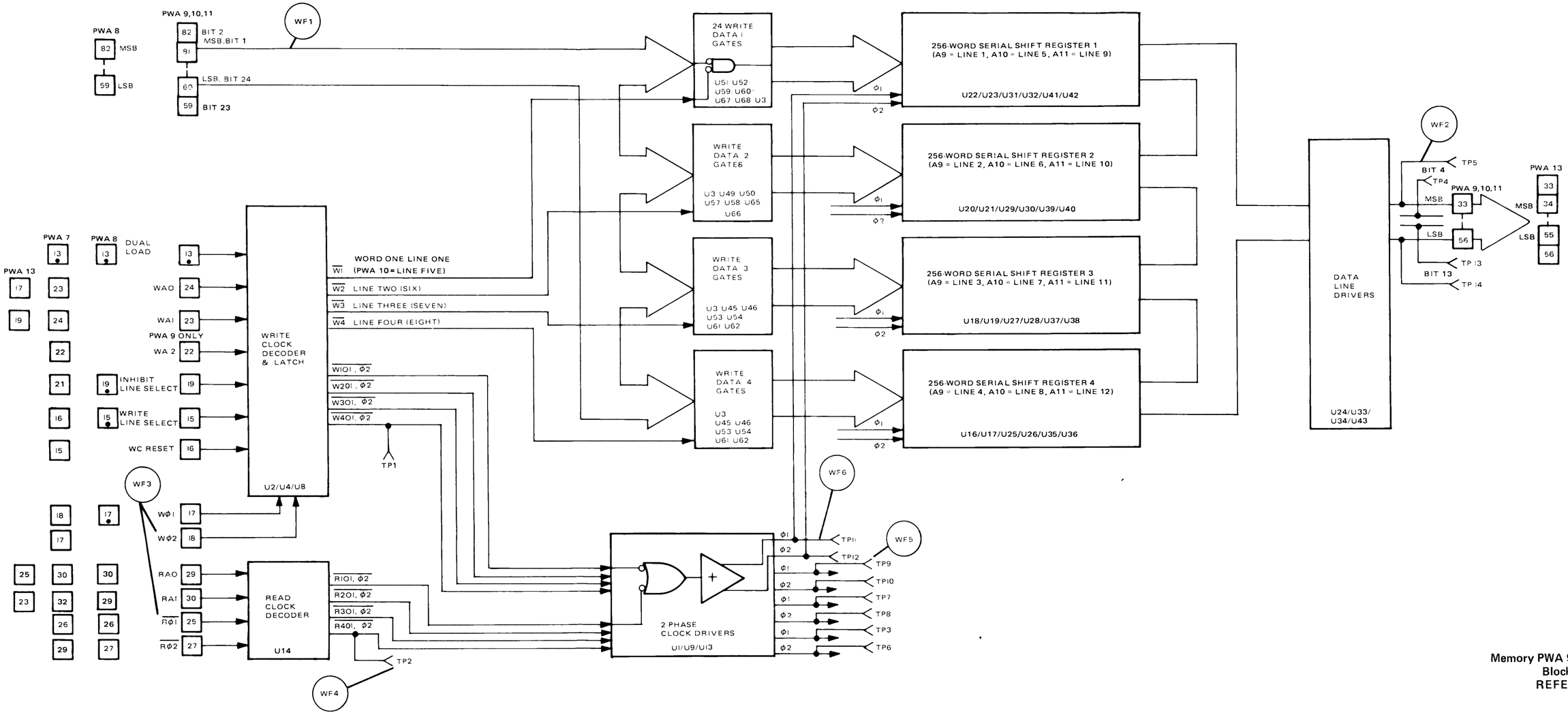


Figure 9-2. Memory Organization Simplified Block Diagram

will lag the corresponding write timing decode (WMA line 1) by six lines. As an example, if PWA 9 line 1 is being loaded, then PWA 11 line 2 is being "read" or unloaded. If tape speed is such that a possibility exists for any given line to be simultaneously accessed for write and read function, an overload signal will be generated. The Memory Control PWA will advance or retard the write address counter two lines to correct for the timing discrepancy. Since this would leave two lines of data empty (white bar on screen), the dual load signal is sent to the write clock decoder in the memory. If line 3 is accessed, lines 1 and 3 are loaded in parallel. When line 4 is accessed, lines 2 and 4 are filled in parallel. The dual load is removed and normal sequencing is resumed until another overload is generated.

9-6. MAINTENANCE

There are no adjustments on the Memory PWA's. Refer to Paragraph 3-21 *Digital Path Faults* in the *System Maintenance* section (Part I) for notes on fault isolation.



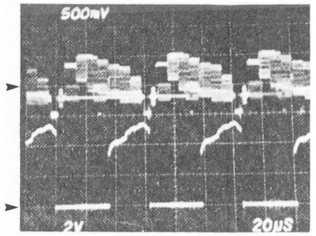
Memory PWA 9 (10, 11)
Block Diagram
REFERENCE 1

A

VIDEO INPUT
PWA 3 TP1

PWA 8 PIN 81
BIT 1 (MSB)
DATA INPUT

WF1



B

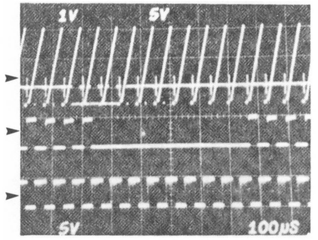
VIDEO INPUT PWA 3
TEST RAMP TP1

U23-1
U52-13 SIMULATE
MISSING BIT
BIT 1 (MSB) SHIFT
REGISTER OUTPUT

WF2

PWA 8 PIN 33
BIT 1 (MSB)
DATA OUTPUT GATE

WF3



C

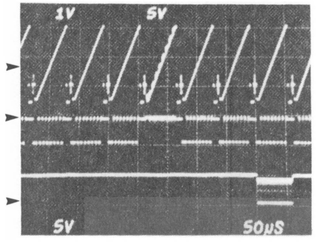
PWA 8 PIN 59 VIDEO
OUTPUT PWA 14 TEST RAMP

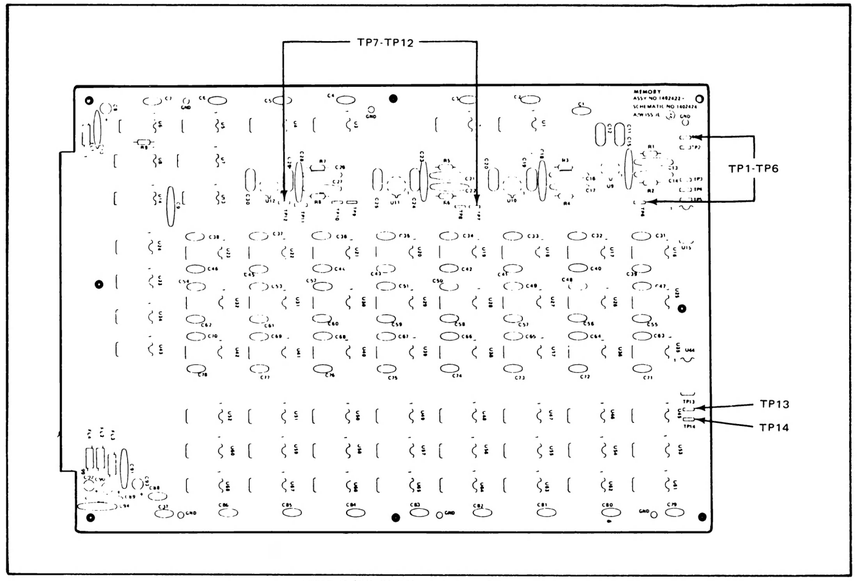
BIT 20 DATA OUTPUT
GATE

WF5

TP2 (PWA 9)
R4Ø1 READ CLOCK
(READ LINE 4)

WF6





PWA 9 (10,11) Component Locator

PWA 9 (10,11) Test Points

TEST POINT	FUNCTION
TP1	Write 4 phase 1
TP2	Read 4 phase 1
TP3	Write/read 4 phase 1
TP4	Line 1 through 4 bit 4
TP5	Line 1 through 4 MSB
TP6	Write/read 4 phase 2
TP7	Write/read 3 phase 1
TP8	Write/read 3 phase 2
TP9	Write/read 2 phase 1
TP10	Write/read 2 phase 2
TP11	Write/read 1 phase 1
TP13	Line 1 through 4 LSB
TP14	Line 1 through 4 bit 13

Waveforms, Test Points, Component Locator Memory PWA 9 (10, 11) REFERENCE 2

SECTION 13

P/S CONVERTER VELOCITY COMPENSATOR DESCRIPTION AND MAINTENANCE

13-1. INTRODUCTION

There are two optional P/S Converter PWA's: with and without velocity compensator. The velocity compensator option is covered first.

Refer to the following documents in the *Parts Lists and Schematics* manual:

P/S Converter with Velocity Compensator:

ASSEMBLY No. 1409125

SCHEMATIC No. 1409127

P/S Converter

ASSEMBLY No. 1402396

SCHEMATIC No. 1402427

Numbered data sheets (REFERENCE 1, 2, 3 . . . *n*) to which PWA descriptions and maintenance procedures refer are located at the end of this section as follows (Vel Comp option first):

Overall Block Diagram – REFERENCE 1

Simplified Schematic – REFERENCE 2, 3, 4

Waveforms – REFERENCE 5

Maintenance Data – REFERENCE 6

P/S Converter Block Diagram – REFERENCE 7

Maintenance Data – REFERENCE 8

P/S CONVERTER PWA 13 FUNCTION SUMMARY:

- Using 3:1 multiplexers, converts 3.58-MHz rate 24-bit data to 10.7-MHz 8-bit data for use in D/A converter section of Video Output PWA 14.
- Velocity compensator option compares the sync phase error of each successive H-line, converts the error to an 8-bit binary number, and stores 12 H-lines to line error data corresponding to the 12 video lines in memory. As a line from memory is read, the line error for that line is also read from the velocity compensator error store which is used to modulate the 3.58-MHz read clock.

13-2. DESCRIPTION

13-3. General

Parallel-to-Serial Converter PWA 13 clocks the 24-bit words of digitized video from the Memory PWA's, at Fsc rate, into serial 8-bit words at 3-Fsc rate. The serial sequence of data is sent to the Video Output PWA on a line-by-line basis where it is converted back into analog video. Clocking of the digital information is under control of the Memory Control PWA. The basic process is the same with or without the velocity compensation option. If the option is not installed, the 3.58-MHz reference subcarrier from the Sync Generator PWA is routed, without modulation, to the Memory Control PWA where it is referred to as read Fsc. If the option is installed, the reference subcarrier is phase-modulated to correct for nonlinear errors of tip-to-tape velocity on a line-by-line basis.

13-4. Parallel-to-Serial Conversion. The parallel-to-serial conversion function of assembly no. 1409125 is, with the exception of different reference designators for components, identical to the circuits described in assembly no. 1402396 (reference paragraph 13-15).

13-5. Velocity Errors. Velocity errors are nonlinear time-base errors of the recorded signal due

to a complex combination of factors that affect the rate at which video information is recorded onto and/or read out of the tape on the VTR. The rate of change of error varies from beginning to end of a given line of video (short-term errors), and from beginning to end of a given field (long-term errors). The TBC makes a correction for these errors in the velocity compensation option on a line-by-line basis. Variations in tip-to-tape velocity are minute, but are sufficient to cause a change of hue throughout the frame of displayed color video.

13-6. Velocity Compensation. On a line-by-line basis the velocity error is assumed to be a ramp function for correction purposes. The Tape H Comparator PWA measures the velocity error for a given line of tape signal and forwards that information to the velocity compensation circuits as a line error signal. The velocity compensation option circuits sample this value and store it. The stored value is retrieved from a memory and compared with the value for the following line. The difference value between the two is used to determine the slope and polarity of the output of a ramp generator circuit. The reference 3.58-MHz signal from the Sync Generator PWA is converted to a series of ramps at 3.58-MHz rate. The line error ramp, developed by the velocity compensation circuits as an analog of the line error rate of change, modulates the 3.58-MHz ramp. The resultant output from the voltage comparator is a 3.58-MHz-pulse train which varies in phase as a function of the slope of the line error ramp. The modulated 3.58-MHz signal is used as a clock to develop the read function timing signals in the Memory Control PWA. These timing signals are used for the read function by the Memory, Parallel-to-Serial Converter, and Video Output PWA's. Each succeeding line receives an up-dated line error ramp correction. Thus, long-term errors of the field are corrected line by line.

13-7. TBC Velocity Compensation Circuits

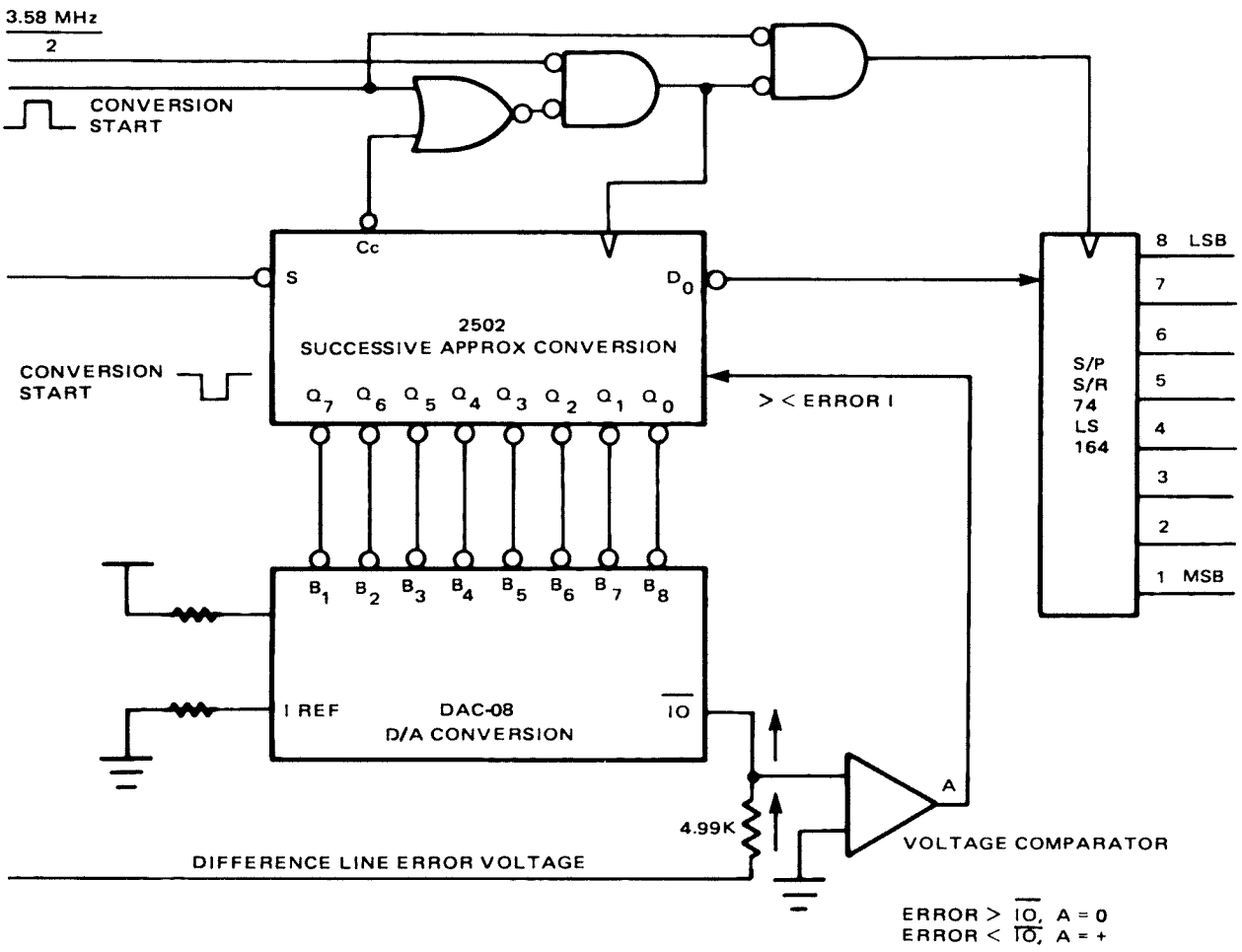
13-8. Functional Description. The TBC stores the off-tape video in a 12-line digital memory on the Memory PWA's. This digital information is read out of the memory in a line-by-line sequence six lines later in time than it is written into the memory. The line error signal is developed in the Tape H Comparator PWA coincident with the memory write operation. To preserve this signal until the corresponding read function for a given line of memory takes place, the velocity compensation option converts the incoming differential line error voltage to an 8-bit digital value and stores it in an 8-bit X 12-line register in the velocity compensation circuits. Timing signals from the Memory Control PWA are encoded to select the line error word in the register that corresponds to the line of digitized video that is being processed by the Parallel-to-Serial Converter PWA. The selected line error word is converted back to analog form and applied to the line error ramp generator. The line error ramp is applied to a voltage comparator as a reference value against the 3-58-MHz ramp signal. The line error ramp "slices" the 3.58-MHz ramps and the resultant output is a phase-modulated 3.58-MHz clock (read Fsc). (See REFERENCE 1, Parallel-to-Serial Converter PWA 13/Velocity Compensation Option, Simplified Block Diagram.)

13-9. Circuit Description.

13-10. *Analog-to-Digital Converter.* Analog-to-digital conversion circuits in the velocity compensation option consist of five integrated circuits:

- 74LS02 steering gates to control the start signal and the 3.58-MHz/2 clock pulses
- successive approximation register
- digital-to-analog converter
- voltage comparator
- serial-to-parallel shift register.

(See Figure 13-1, Differential Line Error Analog-to-Digital Converter.) The DAC-08 outputs current values indicated on the table in the figure as programmed by the digital outputs of the 2502. These currents are summed at one input to the 529 voltage comparator. Reference input of the comparator is at circuit ground. If the error current is more than the D/A $\overline{I/O}$ current, the comparator output is low. If the error current is less than the D/A $\overline{I/O}$ current, the comparator output will be high.



	BINARY WEIGHT	$\overline{IO}$	
	128	1.000 mA	Q_7 = LC
	64	.500 mA	Q_7 = LO
	32	.250 mA	Q_6 = LO
	16	.125 mA	Q_5 = LO
	8	.063 mA	Q_4 = LO
	4	.032 mA	Q_3 = LO
	2	.016 mA	Q_2 = LO
	1	.008 mA	Q_1 = LO
	0	.000 mA	$Q_1^0 \cdot Q_7$ HIGH
TOTAL	256	1.992 mA	I FULL SCALE

Figure 13-1. Differential Line Error Analog-to-Digital Converter PWA 13

Flywheel sync from the Tape VCO PWA is delayed 14 microseconds from the leading edge of H-sync in the write function. This generates a 3.7-microsecond start signal which is reclocked by the 3.58-MHz/2 clock. Master latches of the successive approximation converter are reset by the start pulse. At the first low-to-high transition of the clock pulse after the end of the start pulse, slave latches are set with Q1 through Q6 high and $\overline{Q7}$ low. Bit 1 of the D/A produces a mid-scale $\overline{I/O}$ of 1 mA. If error current is greater than this, the slave latch of Q7 is locked low and a low is clocked into the serial-to-parallel shift register. The next clock pulse sets Q6 low and a similar comparison/shift register entry is made. This action continues until all eight of the binary weighted values have been tried. The complete conversion output stops the clock and triggers two one-shots that perform the next step. One of the one-shots operates the sample-and-hold circuit to store the error voltage for that line so that it may be compared with the value of the next line. The line error voltage has been made at burst crossing time. The next line error voltage is established at burst crossing of the following line. Thus, the differential voltage established represents the accumulated error from the beginning of a line to the end of that line. The other one-shot enables the write address gates to clock the contents of the serial-to-parallel shift register into the 8-bit X12-line storage register.

The read address signals from the Memory Control PWA are encoded to match up the digitized line error signal out of the storage register with the appropriate line of video currently processed by the parallel-to-serial converter circuits. Because the differential line error voltage is read into the storage register one line behind the relevant line of video written into the Memory PWA's, the read address signals are reencoded in the velocity compensation circuits to provide a read address of one line ahead of the read address of the parallel-to-serial (P/S) converter. To express it another way, a given line in the P/S converter arbitrarily designated as line 1 will have the line error data for that line stored in line 2 of the line error storage register. Thus, while line 1 of the P/S converter is accessed, line 2 of the line error storage register must be accessed.

13-11. *Digital-to-Analog Converter.* The RA0' signal from the read address reencoder clocks data out of the 8-bit X 12-line storage register. The RA0', RA1', RA', RB', and RC' signals access appropriate data words in sequence. The D/A converter integrated circuit used here is the same type as was used in the analog-to-digital converter circuit. By placing a resistor on the $\overline{I/O}$ output capable of sourcing 1 mA of current the D/A converter is operated in a bipolar mode. That is, the range of output voltages extends from a positive full-scale output of −10 volts (binary 256 at the digital input), through a midscale zero output, to a negative full-scale output of +10 volts (binary 000 at the digital input). The D/A converter feeds the input of an inverter operational amplifier with a gain of −2.

13-12. *Line Error Ramp Generator.* An FET switch and noninverting voltage follower form a sample-and-hold circuit for the buffered output of the D/A converter. RA0' trips a one-shot (U36-12) that operates the sample-and-hold and dumps the charge on the ramp generator charging capacitor C44. When the one-shot times out, the ramp starts and continues to the end of the video line.

13-13. *Read Fsc Phase Modulator.* Reference Fsc from the Sync Generator PWA clocks a 3.58-MHz rate ramp generator. This waveform is applied to one input of a voltage comparator. The linear error ramp "slices" the 3.58-MHz pulse train which is labeled as read Fsc at the output of the Parallel-to-Serial Converter PWA.

13-14. Second-Order Velocity Error Compensation. Voltage value at the output of the voltage follower U37-1 is an analog of the nonlinear time-base error from the start of a given line to the end of that line. It is derived by measuring the velocity error at the beginning of a line, storing that value, and comparing it with a value obtained from the succeeding line to obtain the difference between the two. The ramp derived from the differential line error voltage and the correction time length is the velocity compensation ramp. The second-order rate of change of velocity error is given as:

$$\frac{d^2 \text{ (velocity error)}}{dt^2}$$

Error amplifier U38-7 generates a waveform which has a symmetrical curvature to satisfy the conditions stated above. It is then added to the first order correction of the error correction ramp generated by U37-7. If there is no second-order rate of change, the linear ramp is not affected. (See Figure 13-2, Second Order Correction Waveforms.) The second-order difference of velocity error is determined by taking the difference between two successive first-order differences in the sample-and-hold difference amplifier U45-1. This second-order difference is integrated and offset by U38-7 to generate a line-rate ramp which is symmetrical about zero. This is then integrated along with the first-order difference in the integrator of the correction ramp generator 37-7.

13-15. Functional Description (1402396)

The Parallel-to-Serial Converter PWA clocks the 24-bit words of digitized video from the Memory PWA's, at Fsc rate, into serial 8-bit words at 3-Fsc rate. The serial sequence of data is sent to the Video Output PWA on a line-by-line basis where it is converted back into analog video. Clocking of the digital information is under control of the Memory Control PWA. The basic process is the same with or without the velocity compensation option. If the option is not installed, the 3.58-MHz reference subcarrier from the Sync Generator PWA is routed, without modulation, to the Memory Control PWA where it is referred to as read Fsc. If the option is installed, the reference subcarrier is processed to correct for nonlinear errors of tip-to-tape velocity on a line-by-line basis.

13-16. Parallel-to-Serial Conversion

(See REFERENCE 7, Parallel-to-Serial Converter without velocity Compensation Option, Block Diagram.) RCB1 and RCB3 from the Memory Control PWA are the clock signals for the conversion process. (See waveforms A and B.) RCB1 clocks the 24-bit data words from the Memory PWA's into a 24-bit register. RCB1 and RCB3 together are an encoded clock that operates the output multiplexer. When RCB1 alone is high, bits 1 through 8 are presented to the output pins of the Parallel-to-Serial Converter PWA. At the next interval, coincident with the next cycle of reference subcarrier, both RCB1 and RCB3 are low; bits 9 through 16 are multiplexed through. Then RCB3 goes high, allowing bits 17 through 24 to appear at the output. The next following RCB1 pulse initiates the sequence for the following 24-bit word. The serial 8-bit values are transformed into analog video signal in the Video Output PWA.

13-17. P/S CONVERTER (VEL COMP) MAINTENANCE

See REFERENCE 5 and REFERENCE 6 at the end of this section for the component locator diagram, jumper/test point/adjustable component summaries, and waveforms called out in these procedures.

Before undertaking any adjustments to the P/S converter velocity compensation circuits, review the *System Alignment Guide* (Table 3-2) and the *Tape/Reference Test Loop* discussion (paragraph 3-5) in the *System Maintenance* section (Part I) for a general understanding of the scope of these field adjustments.

Consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the P/S converter and interactive functions between it and other PWA's before making any adjustments.

This procedure is intended as a check of the basic performance of the velocity compensation option and a method of adjustment for error within the circuit. If problems are suspected after completion of the procedure, substitution of PWA 13 should be used as a troubleshooting aid. Further adjustment requires the use of specialized equipment available only at the factory. If the velocity compensator option is a later addition to the TBC, only the vernier correction gain (R1) need be adjusted as outlined in step 7f.

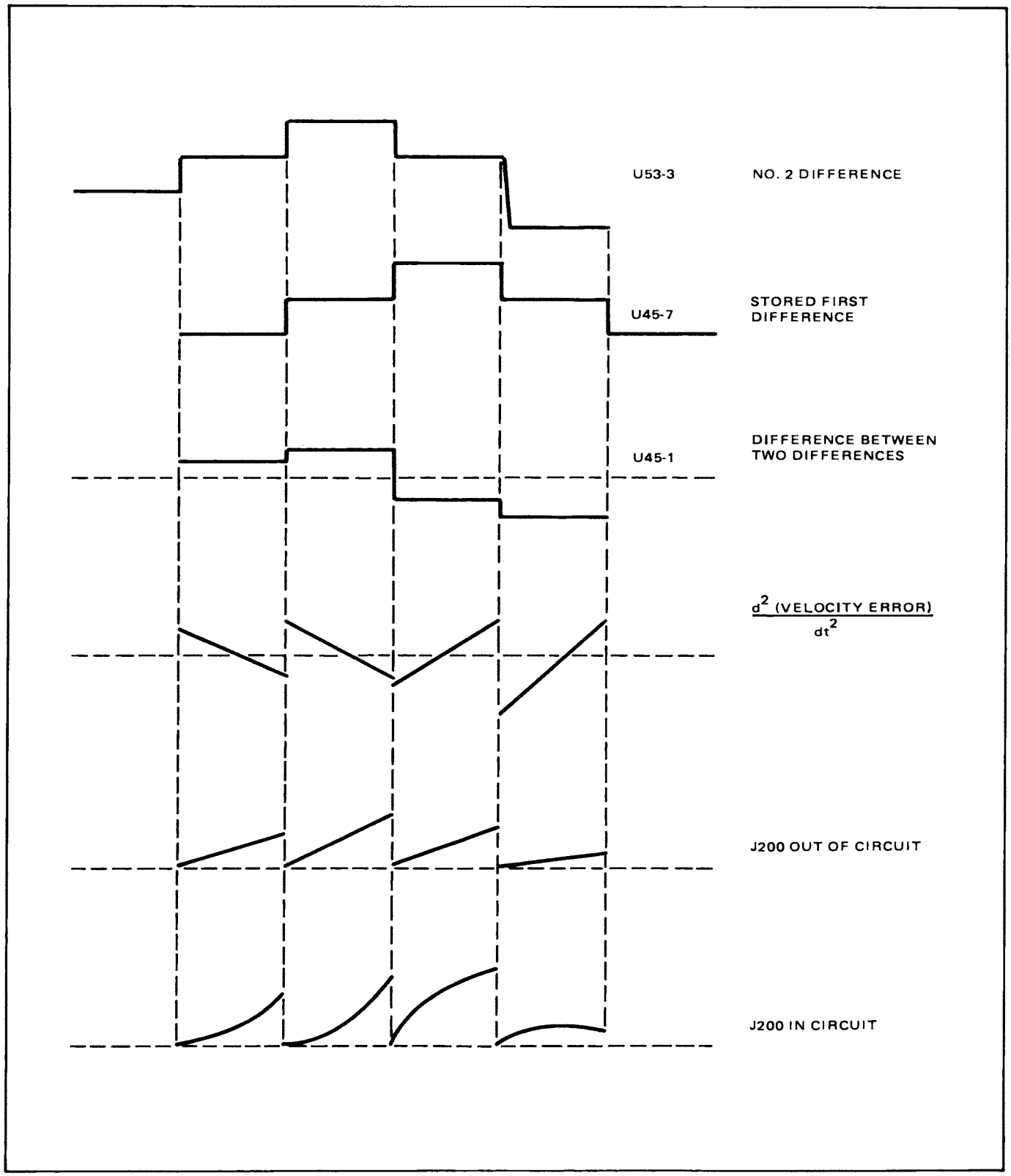


Figure 13-2. Second Order Correction Waveforms, Assembly No. 1409072

13-18. Velocity Compensator Alignment

1. Use the basic tape/reference test loop set-up with a 75% color-bar signal at standard level to TAPE VIDEO IN and a vectorscope at VIDEO OUT 1.

2. With power off extend P/S Converter.

3. Switch velocity compensation on (switch S1 up – PWA edge).

4. Set jumper J1 to B–C (test). (This forces a median value out of the D/A Converter, U52.)

5. Clock ramp generator:

   a. Connect oscilloscope:

      Channel 1: TP21 (clock ramp)

      Trigger: Internal

   b. Adjust R118 (ramp reset) for a ramp with 20 ns off-time at negative edge as shown in WF20(K). If adjustment is not properly made, the clock ramp generator will drift.

6. Input/output offset compensation:

   a. Connect oscilloscope

      Channel 1: TP20 (vel comp ramp)

      Trigger: PWA 13 pin 21 (RMC)

      Typical line-by-line ramps are given in waveform 22 (L).

   b. Adjust R100 (first-order output offset) so that no ramp is visible. Use maximum vertical gain on the oscilloscope.

   c. Connect oscilloscope:

      Channel 1: TP23 (second-order correction)

      Trigger: Pin 83 (flywheel sync)

   d. Adjust R97 (second-order offset) for no ramp.

   e. Return jumper J1 to A–B.

   f. Ground TP2 (line error input).

   g. Return oscilloscope probe to TP20.

   h. Adjust R6 (input offset) for no ramp.

   i. Remove ground on TP2 and disconnect oscilloscope.

7. First-order correction gain and ramp timing:

   a. Connect vectorscope to VIDEO OUT 1.

   b. Misadjust R1 (vernier correction gain) to a 3/4 clockwise position.

   c. Play a recording of 75% color bars.

   d. Adjust R51 (correction start) for a 2.5 (± 10%) μs pulse at the Q3 collector (junction R63/66). Ramps must start between the end of burst and the start of picture video.

   e. Adjust R64 (coarse correction gain) for minimum vector dot size.

   f. Adjust R1 for minimum vector dot size.

   NOTE

   This completes first-order correction adjustments.

8. Second-order correction gain:

   a. Connect oscilloscope:

Channel 1: TP23 (second-order ramp)

Channel 2: PWA pin 83 (flywheel sync)

Trigger: PWA pin 83

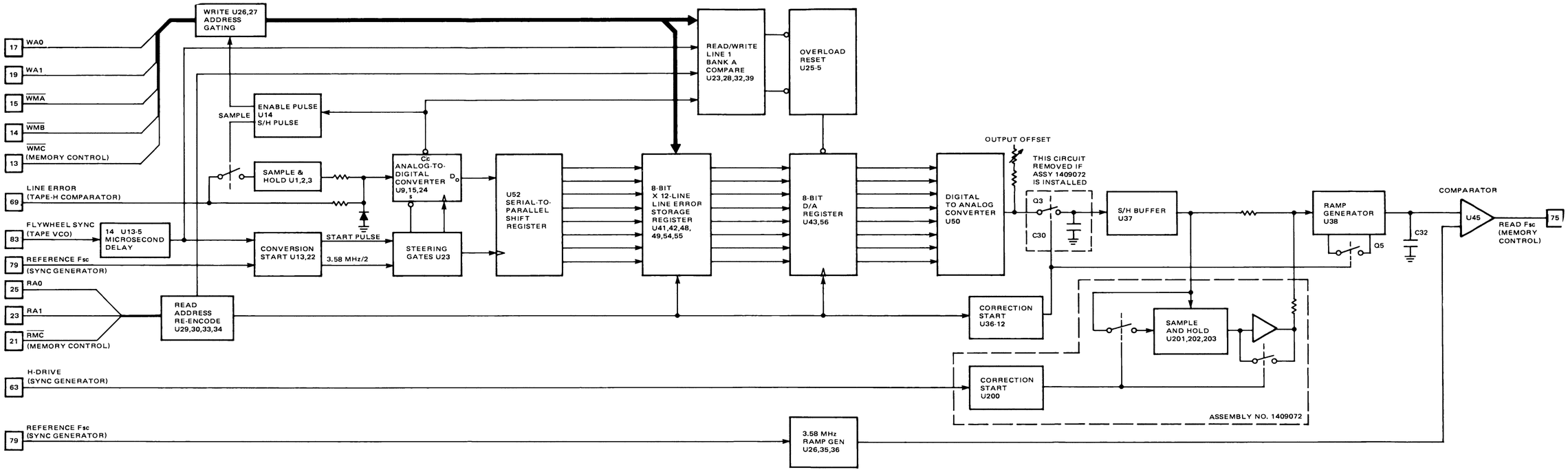
b. Adjust R86 (second-order ramp gain) so that ramps cross zero-volt dc level at the center of the horizontal line as illustrated in WF24(N).

c. Adjust R65 (second-order output gain) for minimum vector dot size.

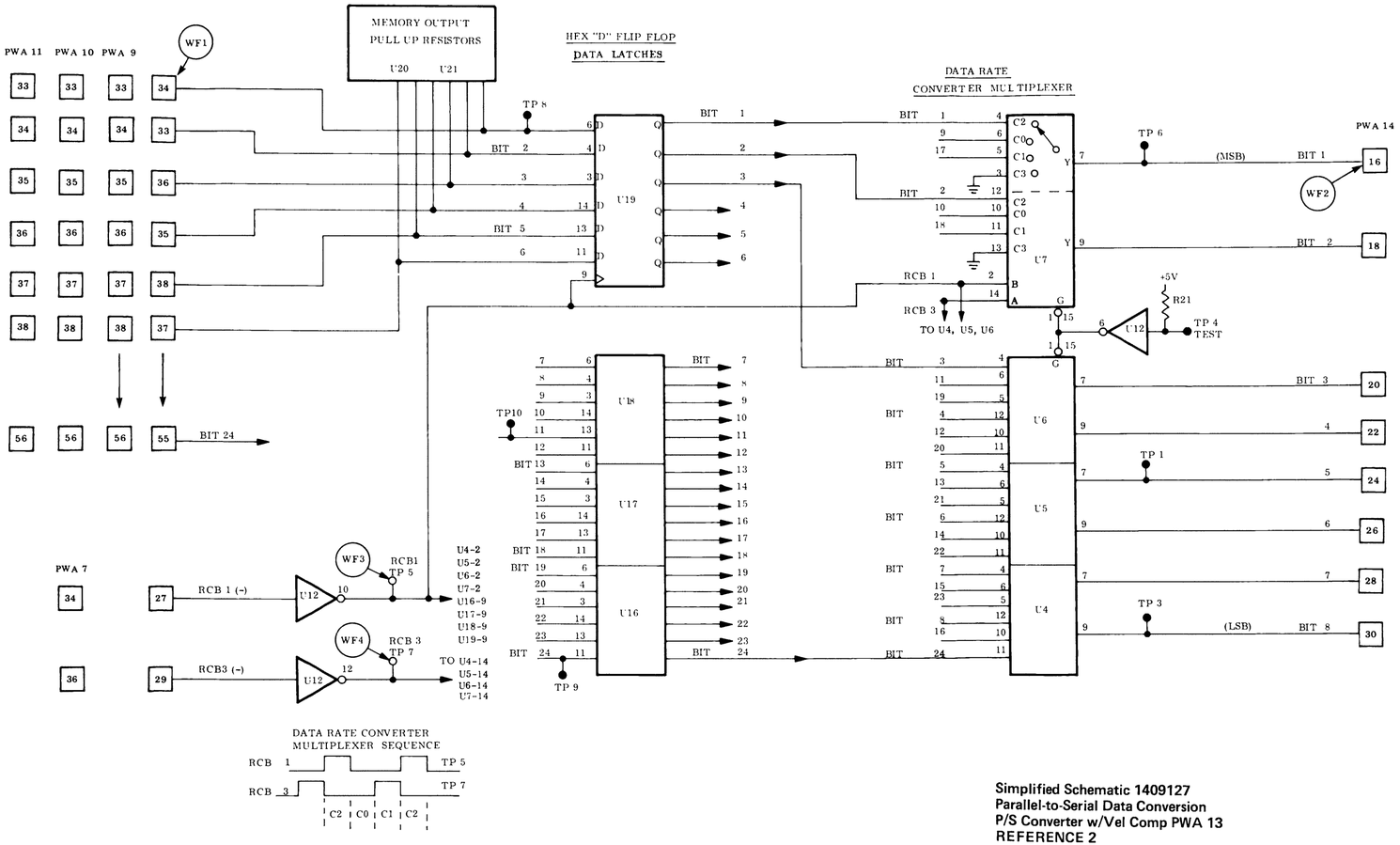
NOTE

Adjustment of R65 should be done with care. It is possible to swamp the first-order correction with the second-order correction gain.

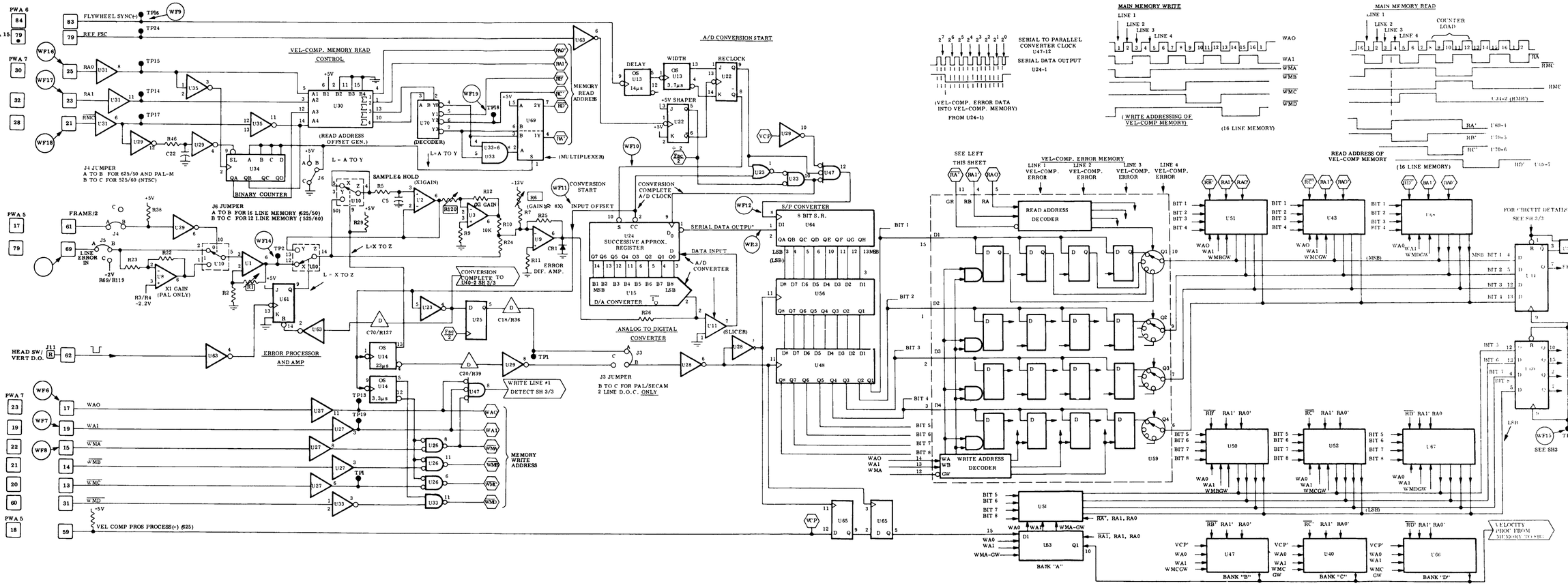
d. With power off, remove PWA from the extender and replace it in the frame.



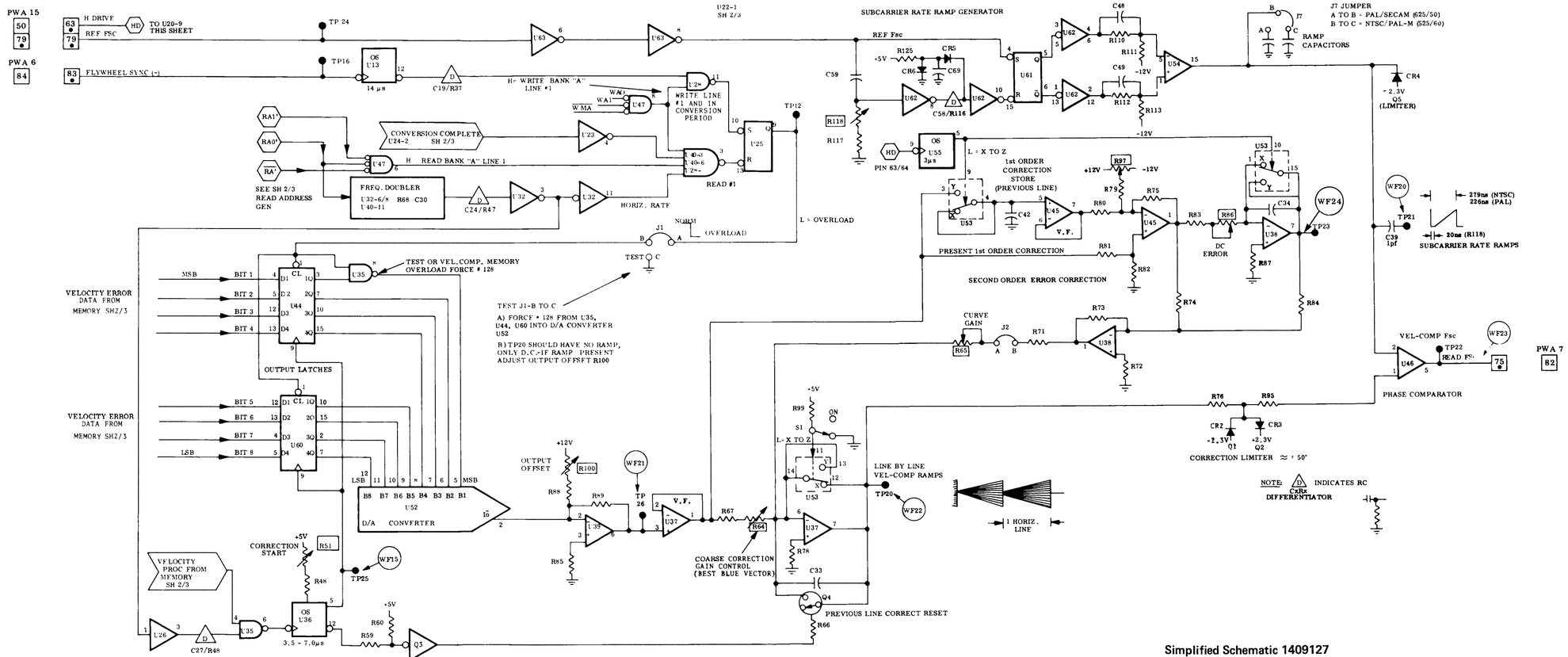
Block Diagram 1409127
Parallel-to-Serial Converter/Velocity Compensation Option, PWA 13
REFERENCE 1



Simplified Schematic 1409127
Parallel-to-Serial Data Conversion
P/S Converter w/Vel Comp PWA 13
REFERENCE 2



Simplified Schematic 1409127
Velocity Error Storage P/S Converter
w/Vel Comp PWA 13
REFERENCE 3

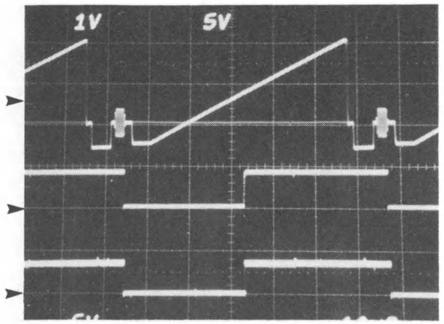


Simplified Schematic 1409127
Velocity Error Output P/S Converter
w/Vel Comp PWA 13
REFERENCE 4

PART II
13-12

AMPEX 1809474-01

A



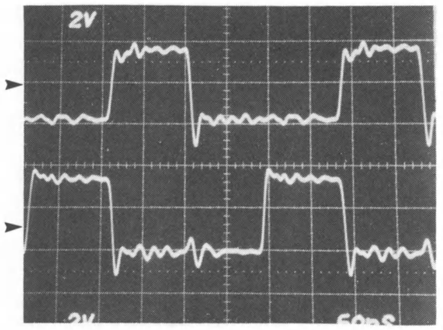
THIS TRACE IS TBC VIDEO OUT 1 PWA 3 RAMP

PIN 34 MSB IN FROM MEMORY — WF1

PIN 16 MSB OUT — WF2

TRIG: PIN 21

B

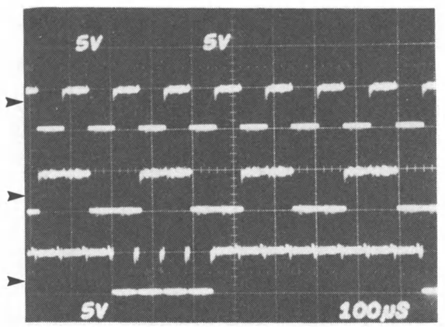


TP5 RCB1 — WF3

TP7 RCB3 — WF4

TRIG: TP 5

C



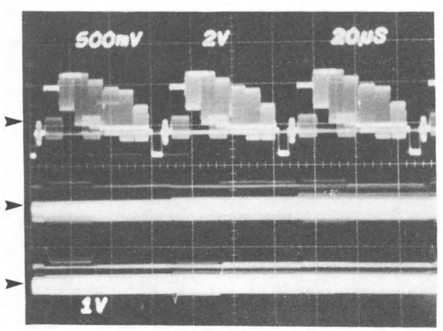
PIN 17 WA0 — WF6

PIN 19 WA1 — WF7

PIN 15 WMA — WF8

TRIG: PWA 10 TP2

D



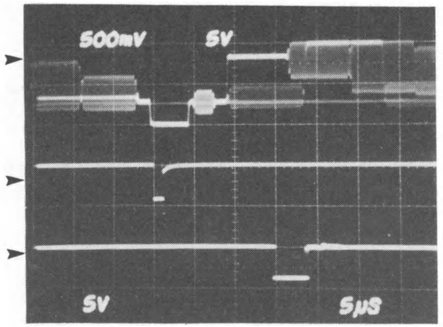
THIS TRACE IS VIDEO INPUT PWA 3 TP1

PIN 69 LINE ERROR IN — WF5

TP2 GAIN CONTROL BUFFER OUTPUT — WF14

TRIG: PIN 17 VPR IN NORMAL PLAY

E



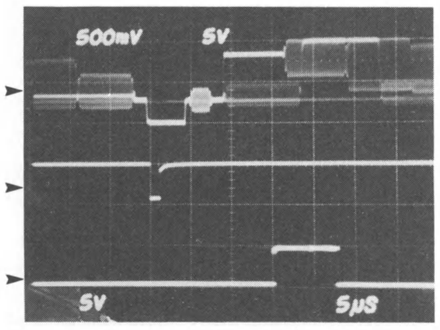
THIS TRACE IS VIDEO INPUT PWA 3 TP1

TP16 FLYWHEEL SYNC — WF9

U24-10 A/D CONVERSION START — WF10

TRIG: TP16

F



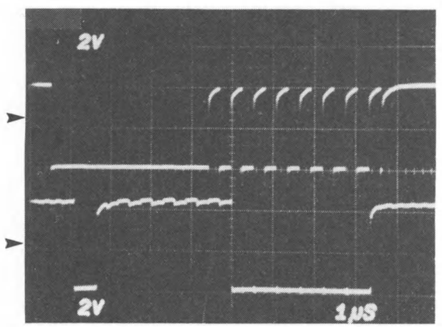
THIS TRACE IS VIDEO INPUT PWA 3 TP1

TP16 FLYWHEEL SYNC — WF9

U24-2 CONVERSION COMPLETE — WF11

TRIG: TP16

G

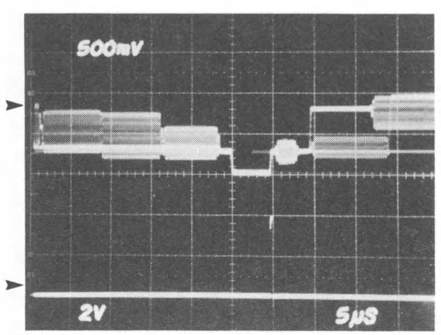


U64-8 S/P CONVERTER (U64) CLOCK — WF12

U64-1 SERIAL DATA U64-1 (BINARY NUMBER 129) — WF13

TRIG: TP16

H

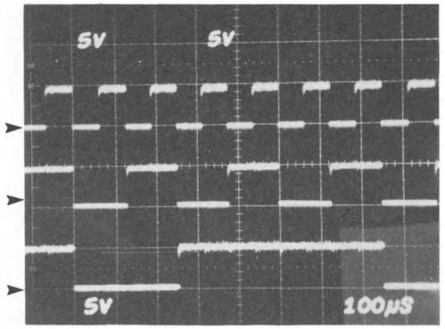


THIS TRACE IS TBC VIDEO OUT 1

TP25 H RATE CONVERTER CLOCK — WF15

TRIG: TP25

I



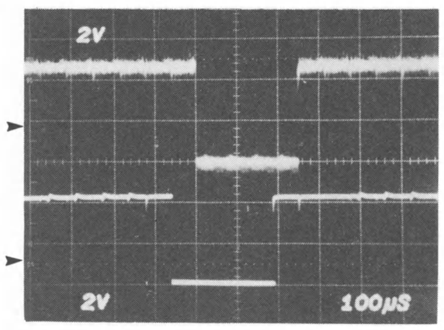
PIN 25 RA0 — WF16

PIN 23 RA1 — WF17

PIN 21 RMC — WF18

TRIG: PIN 21

J

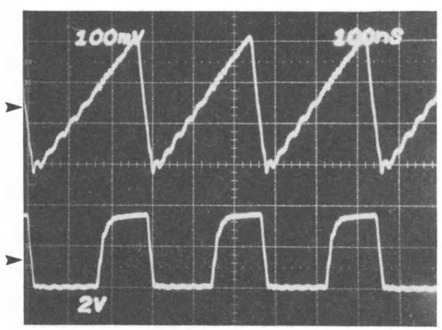


PIN 21 RMC — WF18

TP18 READ MEMORY C — WF19

TRIG: PIN 21

K

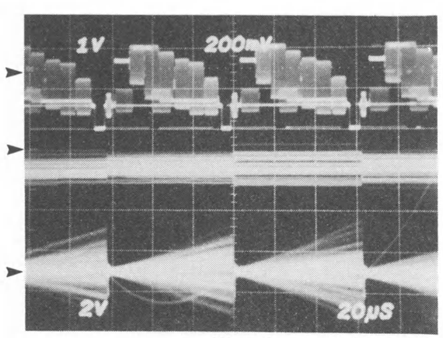


TP21 REFERENCE RAMP — WF20

PIN 75 READ Fsc — WF23

TRIG: PIN 75

L



THIS TRACE IS TBC VIDEO OUT 1

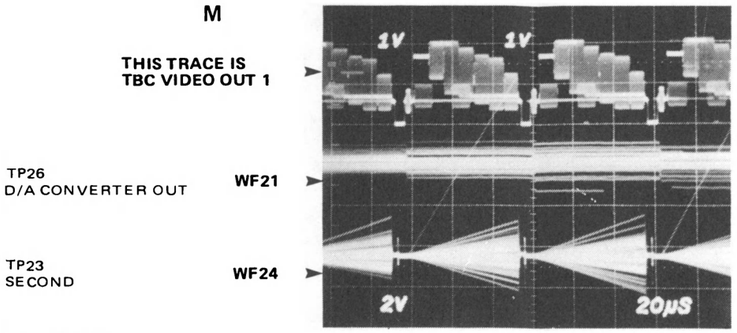
TP26 D/A CONVERTER OUT — WF21

TP20 LINE-BY-LINE VEL COMP RAMP — WF22

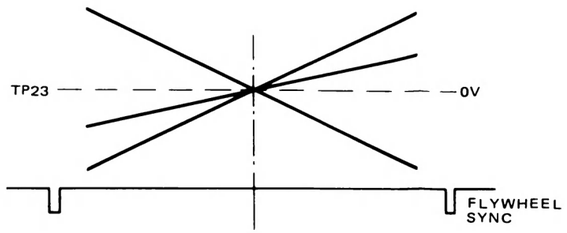
TRIG: PIN 21, VPR IN NORMAL PLAY

Waveforms (1409127)
P/S Converter w/Vel Comp PWA 13
REFERENCE 5

M



TRIG: PIN 21,
VPR IN NORMAL PLAY

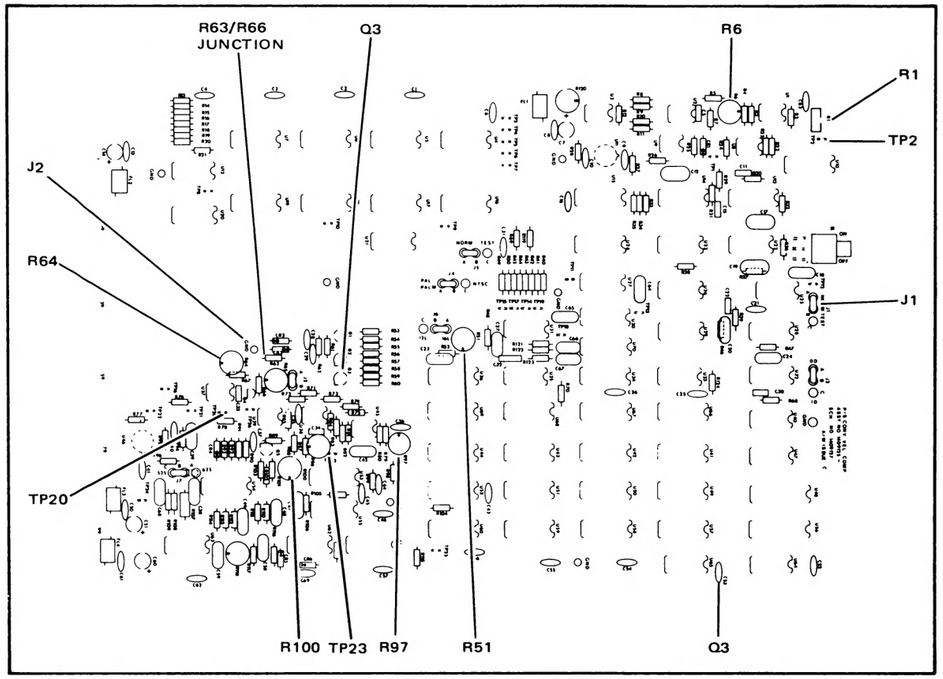


PWA 13 (1409127) Test Points

TEST POINT	NAME
TP1	Error difference
TP2	Processed line error
TP3	LSB
TP4	+5V
TP5	$\overline{\text{RCB1}}$
TP6	MSB
TP7	$\overline{\text{RCB3}}$
TP8	MSB byte 1
TP9	LSB byte 3
TP10	3rd MSB byte 2
TP11	$\overline{\text{WMC}}$
TP12	Memory overload
TP13	Write address zero
TP14	Read address one
TP15	Read address zero
TP16	Flywheel sync
TP17	$\overline{\text{RMC}}$
TP18	Read memory C
TP19	Write address one
TP20	Correction ramps
TP21	Reference ramps
TP22	Read Fsc
TP23	2nd order correction
TP24	Reference Fsc
TP25	H rate clock
TP26	D/A converter out

PWA 13 (1409127) Jumpers

JUMPER	POSITION – FUNCTION	
J1		
	A–B	Normal
	B–C	Test – forces memory overload condition
J2		
	A–B	Normal
	Removed	Disconnects second order correction
J3		
	A–B	NTSC – 5-1/2 line advance
	B–C	PAL/SECAM – 7-1/2 line advance
J4		
	A–B	PAL/SECAM
	B–C	NTSC
J5		
	A–B	Normal
	B–C	Test – inserts fixed error voltage
J6		
	A–B	16-line memory
	B–C	12-line memory
J7		
	A–B	PAL/SECAM
	B–C	NTSC/PAL-M

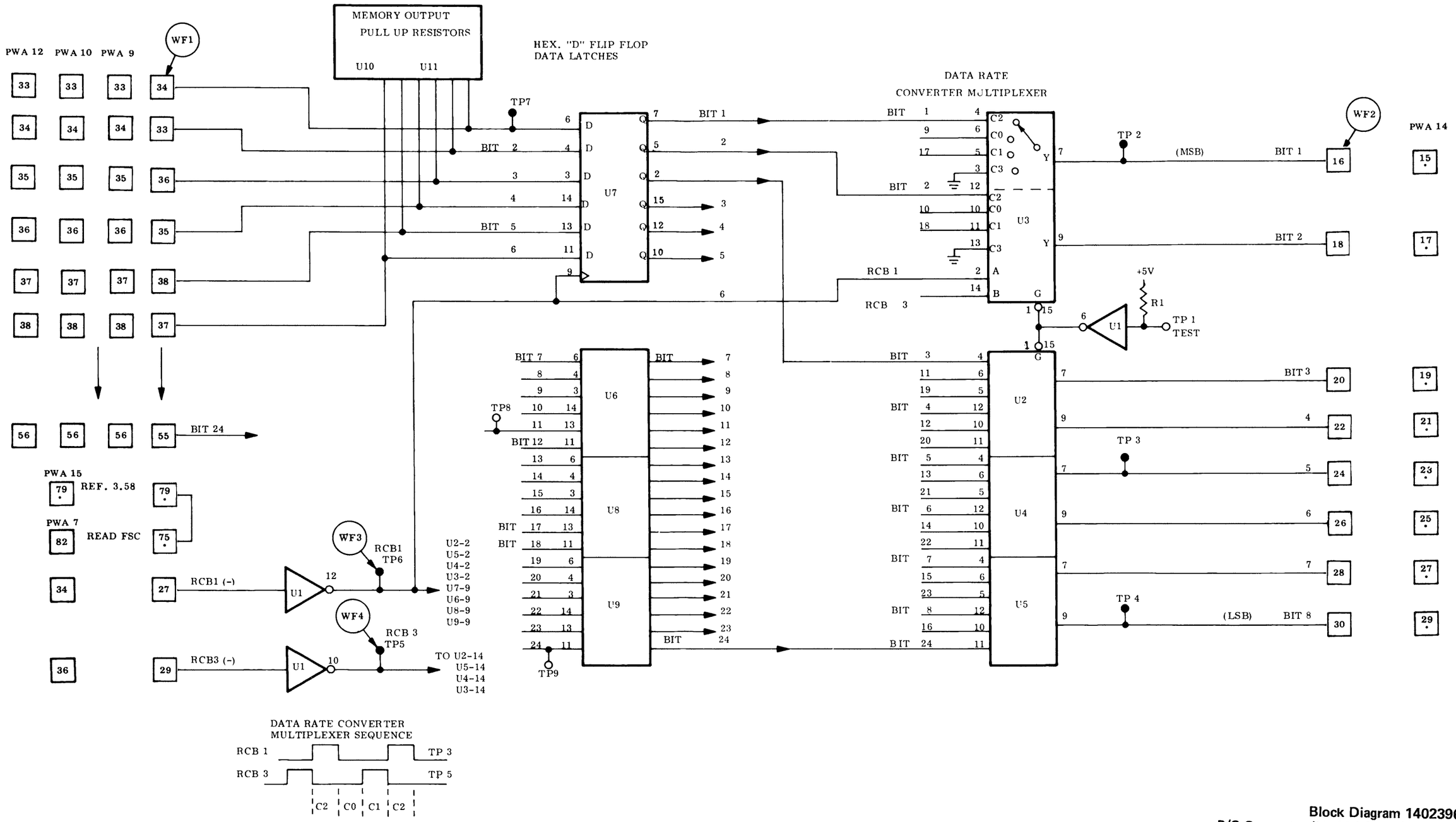


PWA 13 (1409127) Component Locator

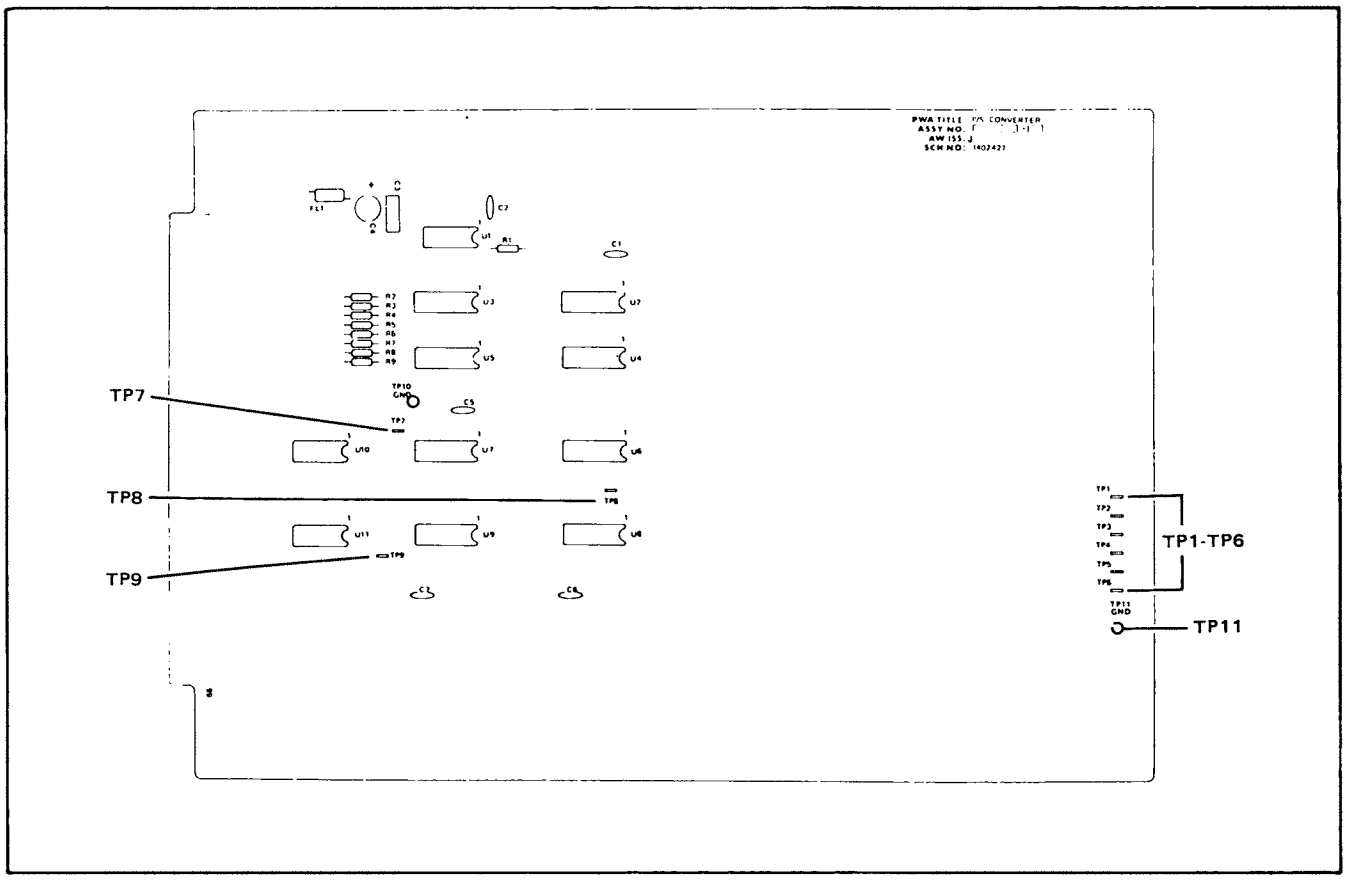
PWA 13 (1409127) Adjustable Components

COMPONENT	FUNCTION
R1	Vernier correction gain
R6	Input offset
R51	Correction start
R64	Coarse correction gain
R65(1)	Curve gain
R86(1)	DC error
R97	2nd order offset
R100	Output offset
R118(1)	Ramp delay
R120(2)	Loop gain
S1	Vel comp on/off

(1) FACTORY ADJUST ONLY
(2) NOT USED IN NTSC



Block Diagram 1402396
P/S Converter (No Vel Comp) PWA 13
REFERENCE 7



PWA 13 (1402396) Component Locator

PWA 13 (1403296) Test Points

TEST POINT	NAME
TP1	+5V
TP2	MSB
TP3	5th MSB
TP4	LSB
TP5	Read clock byte 3
TP6	Read Clock byte 1
TP7	MSB byte 1
TP8	3rd MSB byte 2
TP9	LSB byte 3
TP10	Ground
TP11	Ground

Component Locator Test Points
P/S Converter (No Vel Comp) PWA 13
REFERENCE 8

SECTION 14

VIDEO OUTPUT

DESCRIPTION AND MAINTENANCE

14-1. INTRODUCTION

Refer to the following documents in the *Parts Lists and Schematics* manual:

ASSEMBLY No. 1405189

SCHEMATIC No. 1405191

Numbered data sheets (REFERENCE 1, 2, 3 . . . *n*) to which PWA descriptions and maintenance procedures refer are located at the end of this section as follows:

Overall Block Diagram – REFERENCE 1

Simplified Schematic – REFERENCE 2

Waveforms – REFERENCE 3

Maintenance Data – REFERENCE 4

VIDEO OUTPUT PWA 14
FUNCTION SUMMARY:

- Provides digital-to-analog conversion of the serial 8-bit data from P/S Converter PWA 13 back to analog video.
- During blanking interval the D/A conversion circuits are preset to the binary equivalent of the blanking level, yielding an analog video signal referenced to blanking.
- The analog video is filtered and clamped to the reference black level.
- Adds sync, burst, and reference timing from the Sync Generator PWA 15 to the time-base-corrected video.
- Provides three outputs. VIDEO OUT 1 and TBC video (for monitoring) are composite video; VIDEO OUT 2 sync can be inhibited by jumper positioning.

14-2. DESCRIPTION

The Video Output PWA accepts 8-bit data words from the Parallel-to-Serial Converter PWA 13 and converts them into analog video. In addition, horizontal and vertical sync, blanking, and burst, slaved to station master video, are reinserted in the video to form composite video and complete the time-base correction process. Video output drivers no. 1 and no. 2 provide a 1-volt-each peak-to-peak composite video signal (into 75 ohms) to coaxial jacks at the rear panel of the TBC. Video output driver no. 1 also provides composite video to the Video Processor PWA 16. If the Video Processor option is not installed, jumper J2 (on the backplane of the TBC) routes the signal to the Video Input PWA 3.

14-3. Digital-to-Analog Conversion

Serial 8-bit data words are clocked into the input latch by reference 3 Fsc. The clocking process is inhibited during horizontal and vertical blanking periods by the blanking rise time control circuits. (See REFERENCE 1, Video Output PWA 14, Simplified Block Diagram.) Latched data bits are applied to the D/A converter which converts the digital value to an equivalent value of output current which is supplied to the buffer amplifier.

14-4. Analog Video Processing Circuits

Vertical and horizontal blanking from the Sync Generator PWA 15 is inserted into the quantized video signal by blanking rise time control circuits in the buffer amplifier. To eliminate "spurs" (spurious oscillations) that occur during transition from one quantized value to the next, the

sample-and-hold circuit reads the quantized value after the signal has settled to a true value. In the next stage, horizontal blanking is clamped to ground to establish a reference level for the video signal. Low-pass and sin X/X filtering smooth the steps of the quantized video. The amplitude equalizing amplifier boosts the video to compensate for losses in video processing circuitry. The below-black-level noise clip amplifier removes any noise present in blanking intervals prior to reinsertion of vertical and horizontal sync, and burst.

14-5. Composite Sync and Burst

Burst flag gates subcarrier into the burst shaper. These signals are from the Sync Generator PWA. The burst shaper contours the envelope of the 3.58-MHz burst. The sync shaper controls the rise and fall times of composite sync from the Sync Generator PWA.

14-6. Inhibit White Line Circuit

Bits 1 through 8 from the Parallel-to-Serial Converter PWA are decoded in the inhibit white line circuit to produce a flag if all "1's" are present (white line). During the vertical blanking interval or when in search mode, the flag produces an inhibit to the output video amplifiers. When this inhibit is present, the output of the video amplifiers is clamped to a level close to the black level of horizontal blanking. This circuit is required because in "freeze" mode two and three lines of video are alternately deleted from each field; and, in search, the write clock is randomly advanced or retarded to delete or add lines of video to maintain a recognizable picture on the monitor. Both of these events may cause white line conditions. Thus, video output is attenuated.

14-7. Output Video Amplifier

The reconstituted analog video, sync, burst, and white line inhibit are mixed in the output video amplifiers to produce a composite video signal which is time-base corrected and will deliver a 1-volt peak-to-peak signal into a 75-ohm impedance.

14-8. VIDEO OUTPUT MAINTENANCE

See REFERENCE 3 and REFERENCE 4 in this section for the component locator diagram, jumper/test-point/adjustable-component summaries, and waveforms called out in these procedures.

Before undertaking any adjustments to the Video Output PWA, review the *System Alignment Guide* (Table 3-2) and the *Tape/Reference Test Loop* discussion (paragraph 3-5) in the *System Maintenance* section (Part I) for a general understanding of the nature and scope of these field adjustments.

Consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the interactive functions between the Video Output PWA and other PWA's before making any adjustments.

14-9. Blanking Filter

1. Use basic tape/reference test loop setup with a 0% APL flat field test signal to TAPE VIDEO IN.

2. With power off put Video Output PWA on the extender.

3. Connect oscilloscope to the junction of R125 and R126. Trigger on PWA pin 71.

4. Adjust R55 (blanking level dc balance) so that there is no step in the video at blanking.

5. Adjust signal generator to 50% APL flat field.

6. Connect oscilloscope (terminated) to PWA pin 59 (or VIDEO OUT 1). Trigger on PWA pin 49.

7. Adjust L4 and L5 (blanking insertion filters) for a smooth transition and a fall time of 275 (±30) nanoseconds from the 50% APL level to blanking.

8. Adjust R65 (blanking insertion level) to obtain rounded corners (minimum pre-shoot and overshoot) at the video/blanking insertion level.

NOTE

Beware that the H-blanking leading and trailing edge (R46 and R45 on PWA 15) settings may interfere with adjustment of R65 – appearing as ringing at the video/blanking level transition.

14-10. Sync Levels

1. Use basic tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN.

2. With power off put the Video Output PWA on the extender.

3. Connect oscilloscope to VIDEO OUT 1, trigger on pin 49.

4. Adjust R192 (sync level) for 286 mV.

5. Adjust R221 (burst level) for 286 mV.

6. Adjust R206 (burst balance) so that burst is symmetrical with respect to blanking.

14-11. White Bar Suppression Clamp

1. Use the basic tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN.

2. With power off, put Video Output PWA on the extender.

3. Connect oscilloscope to VIDEO OUT 1 (terminated); trigger on pin 49. Display vertical interval.

4. Misadjust R320 (vertical clamp timing) fully clockwise.

5. With power off, pull Memory PWA 9 out just enough to disconnect it from the mother-board. This "empty memory" produces a white bar.

6. Adjust R314 (vertical clamp level) so that the offset of "white bar" video in the vertical interval is 10 IRE units (75 mV) above blanking level.

7. With power off reinsert Memory PWA 9.

8. Connect oscilloscope –

   Channel 1: U20 pin 12

   Channel 2: PWA pin 72

   Trigger: PWA pin 49

9. Adjust R320 so that positive edge of the pulse at U20 pin 12 is coincident with positive edge of vertical blanking at PWA pin 72 as shown in WF14/15(I).

NOTE

This adjustment depends on the user's setting for R65 (PWA edge SLOW MOTION V BLKG) on the Sync Generator which users may adjust for a particular line in the vertical interval. In this case, R65 should blank out line 16 through its pedestal.

14-12. Black Clip

1. Use the basic tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN.

2. Connect oscilloscope to VIDEO OUT 1 (terminated); trigger on pin 49.

3. With power off put the Video Output PWA on the extender and activate the test ramp with Video Input PWA 3 jumper J4 set to B–C.

4. Adjust R135 (black clip) so that the negative clipping point of the ramp is 35 mV below blanking. The clipped ramp may be seen in WF13(D).

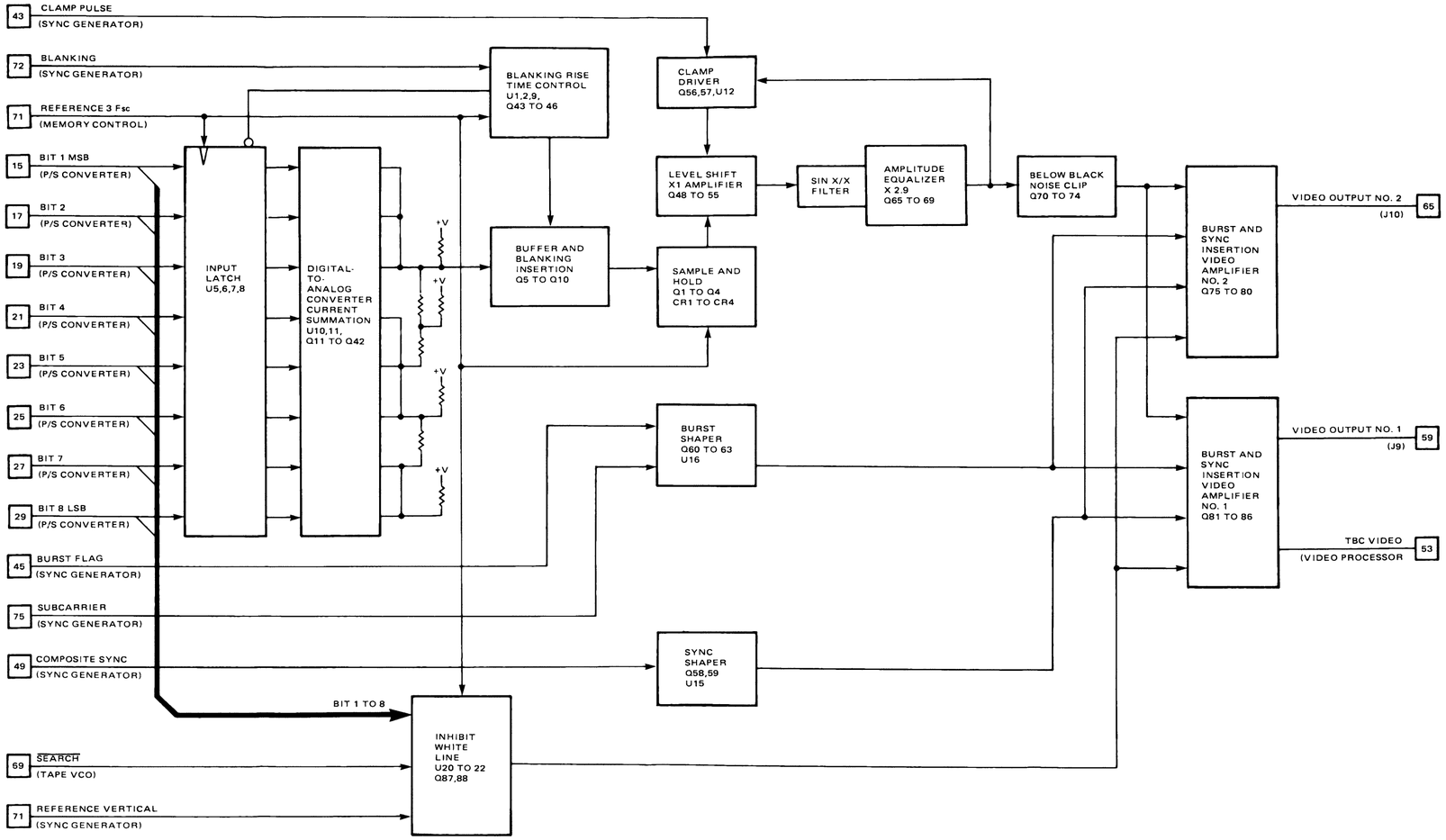
5. Remove PWA 14 J4 and verify that the negative point of the ramp is not clipped. Replace J4.

6. With power off return PWA 3 J4 to A–B and PWA 14 to its slot.

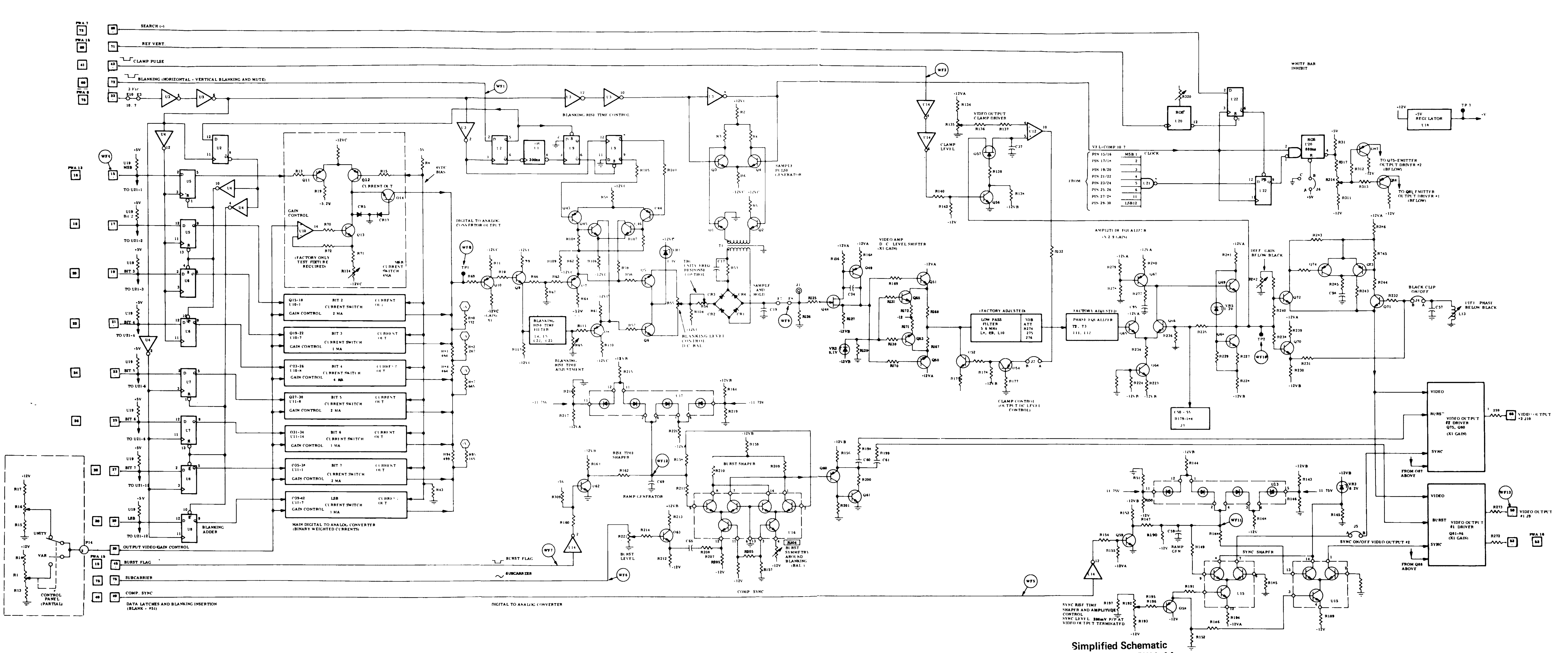
7. Re-check system unity gain.

4-13. Interpolation Filter

The interpolation filter (C80, C83, L8, L9, L10, L11, L12, T2 and T3), the D/A converter (R114, R115, R116, R117, R122 and R123) and the differential gain below black (L13 and R282) are factory aligned to very high tolerances using special test fixtures and measuring devices. These circuits should not be aligned in the field.



Block Diagram
Video Output PWA 14
REFERENCE 1



Simplified Schematic
Video Output PWA 14
REFERENCE 2

PART II
14-6

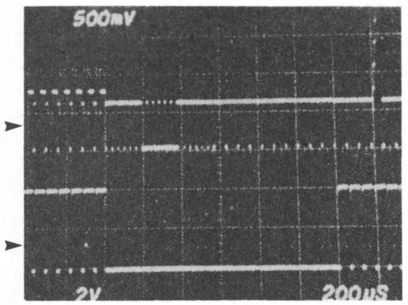
AMPEX 1809474-01

A

PIN 59
VIDEO OUT 1 — WF13

PIN 71
REFERENCE
VERTICAL — WF1

TRIG: PWA 3 PIN 58



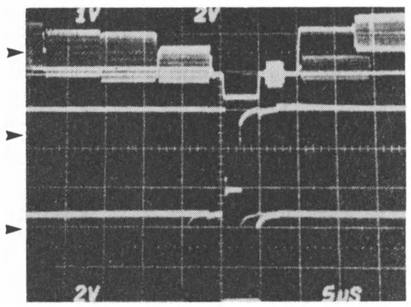
B

PIN 59
VIDEO OUT 1 — WF13

PIN 43
CLAMP PULSE — WF2

PIN 49
COMPOSITE
SYNC — WF5

TRIG: PIN 43



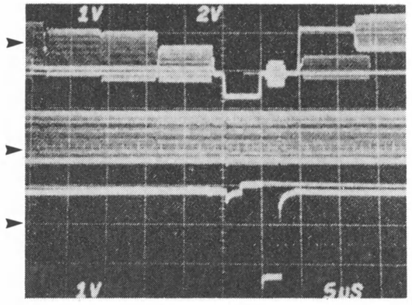
C

PIN 59
VIDEO OUT 1 — WF13

PIN 75
SUBCARRIER — WF6

PIN 45
BURST FLAG — WF7

TRIG: PIN 43



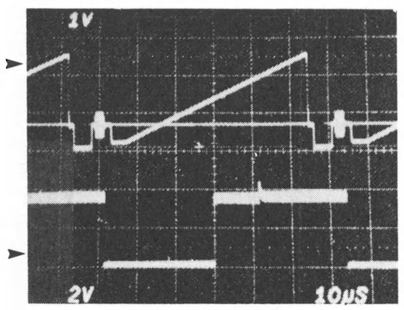
D

PIN 59
VIDEO OUT 1 — WF13

INSERT TEST RAMP:
PWA 3 J4 B–C
DISABLE BLACK CLIP:
PWA 14 J4 REMOVED

PIN 15
BIT 1 MSB — WF4

TRIG: PIN 43

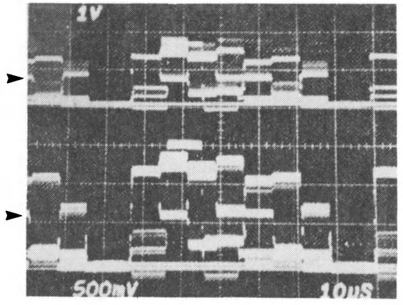


E

TP1
DIGITAL-TO-
ANALOG
OUTPUT — WF8

E7-E8 JUMPER
SAMPLE AND
HOLD OUTPUT — WF9

TRIG: PIN 43

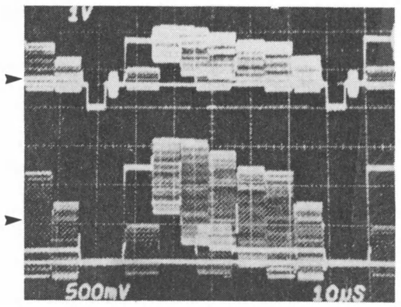


F

PIN 59
VIDEO OUT 1 — WF13

TP2
AMPLITUDE
EQUALIZER
OUTPUT — WF10

TRIG: PIN 43

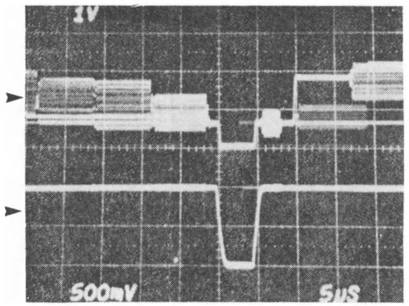


G

PIN 59
VIDEO OUT 1 — WF13

U13-2
SYNC SHAPER
GENERATOR — WF11

TRIG: PIN 43

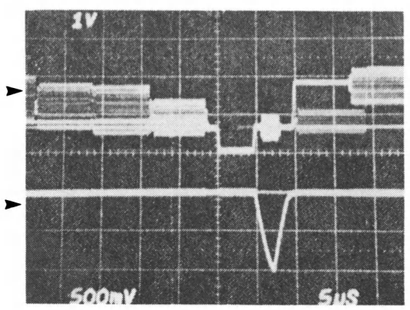


H

PIN 59
VIDEO OUT 1 — WF13

U17-2
BURST FLAG
RISE TIME
SHAPER — WF12

TRIG: PIN 43

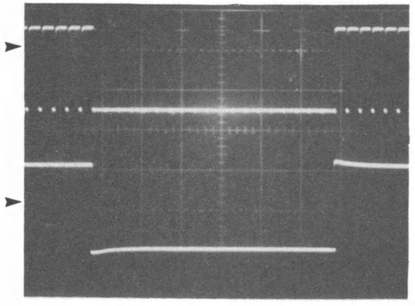


I

U20-12
REFERENCE
VERTICAL — WF14

PIN 72
VERT
BLANKING — WF15

TRIG: PIN 72



PWA 14 Adjustable Components

COMPONENT	LOCATION
C80 (1)	Interpolation filter
C83 (1)	Interpolation filter
L4	Blanking insertion filter
L5	Blanking insertion filter
L8	Interpolation filter
L9	Interpolation filter
L10	Interpolation filter
L11 (1)	Interpolation filter
L12	Interpolation filter
L13	Differential phase below black
R54 (2)	Frequency response
R55	DC balance
R65	Blanking insertion level
R114	MSB gain
R115	2nd MSB gain
R116 (1)	3rd MSB gain
R117	4th MSB gain
R119	5th MSB gain
R122 (1)	6th MSB gain
R123 (1)	7th MSB gain
R135	Black clip
R192	Sync level
R206	Burst balance
R221	Burst level
R282 (1)	Differential gain below black
R314	Vertical clamp level
R320	Vertical clamp timing
T2 (1)	Interpolation filter
T3 (1)	Interpolation filter

(1) Factory adjustment only.

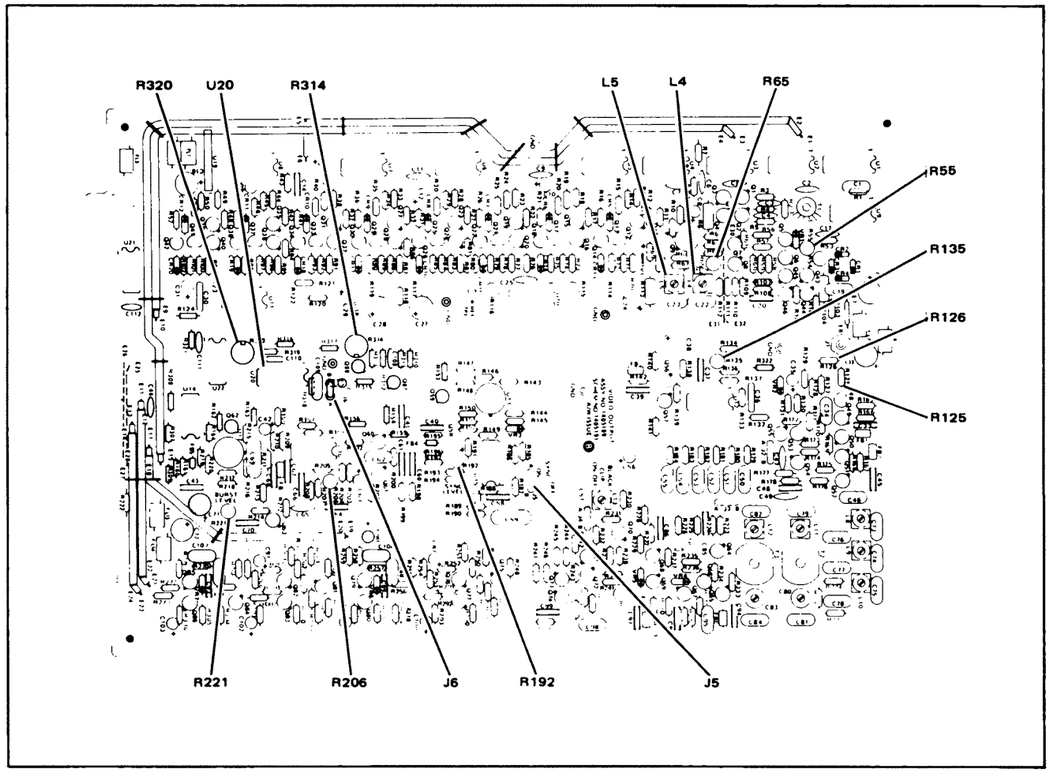
(2) R54 adjusts the high end frequency response (chroma level) and should only be adjusted using a spectrum analyzer with 0.1 dB accuracy.

PWA 14 Test Points

TEST POINT	SIGNAL
TP1	D/A video
TP2	Non-comp video
TP3	+5V

PWA 14 Jumpers

JUMPER	POSITION	FUNCTION
J1	RF connector	Test only – insert sweep to interpolation filter
J2	A–B	Normal
	Removed	Test – removes clamp pulse
J3	A–B	Normal
	Removed	Test – removes phase equalizer
J4	A–B	Normal black clip on
	Removed	Test – removes black clip
J5	A–B	Normal – composite sync on VIDEO OUT 2
	Removed	No composite sync on VIDEO OUT 2
J6	A–B	Normal – Inhibits V interval clamp
	B–C	Test – Disables auto black



PWA 14 Component Locator

Adjustable Components Test Points
Component Locator Jumpers
Video Output PWA 14
REFERENCE 4

SECTION 15

SYNC GENERATOR
DESCRIPTION AND MAINTENANCE

15-1. INTRODUCTION

Refer to the following documents in the *Parts Lists and Schematics* manual:

ASSEMBLY No. 1405186

SCHEMATIC No. 1405146

Numbered data sheets (REFERENCE 1, 2, 3 . . . *n*) to which PWA descriptions and maintenance procedures refer are located at the end of this section as follows:

Overall Block Diagram – REFERENCE 1, 2

Simplified Schematic – REFERENCE 3, 4, 5, 6

Waveforms – REFERENCE 7, 8

Maintenance – REFERENCE 9

SYNC GENERATOR
PWA 15 FUNCTION SUMMARY

- Using reference video input, develops composite sync, burst key, and blanking signals for insertion in the time-base-corrected video at Video Output PWA 14.
- 14.3-MHz LC (for monochrome and nonservoed capstan modes of operation) and crystal (for all other modes) oscillators are the source for two TV sync generator IC's (normal and advanced sync) as well as the analog 3.58 MHz to Video Output PWA 14 and TTL 3.58 MHz to Memory Control PWA 6 by way of velocity compensator on PWA 13.
- The 14.3-MHz oscillators are genlocked by an error signal which results from digital comparison of H-rate sync with the burst position.
- A separate loop with its own TV sync generator IC provides advanced reference sync for VTR's that do not have internal capability for both fixed and floating 5-1/2-line advance. Floating 5-1/2-line advance is mainly used on units using tach lock drum servos.

15-2. DESCRIPTION

Sync Generator PWA 15 produces the read timing signals that recover digitized video from memory at reference 3 Fsc rate. Off-tape video is digitized and entered in memory at the tape velocity rate. Reading data out of memory at a reference rate is the basis of the digital time-base correction process. In addition, the Sync Generator PWA produces horizontal and vertical sync, blanking, and burst. These are inserted into the time-base-corrected analog video in the Video Output PWA 14 to form the composite video output of the TBC.

The Sync Generator PWA contains three basic functional areas: reference video processing, reference oscillator/control processing, and output sync and blanking. This breakdown is shown in REFERENCES 1 and 2, *Overall Block Diagram.* The first area, reference processing, is the top portion of REFERENCE 1. Here, reference video is processed to extract the basic timing signals (burst crossing, H sync, vertical color frame) for the servo loops within the Sync Generator. This simplified block diagram is a rough outline of the detailed circuits given in REFERENCE 3. The bottom half of REFERENCE 1 shows the 14.3-MHz reference oscillator which becomes the source for the read timing signals to the TBC. Note here that the control panel controls at the left are part of the basic servo loop of which the phase comparator, the 14.3-MHz

oscillator, and the sync generator IC (REFERENCE 5) are the central elements. Observe that the signal HD2 (hexagon symbol – horizontal drive) at the input to the phase comparator is from the sync generator IC, and that the signal 130H (hex) is the 2-MHz clock for that IC. This is the basic phase comparator loop around which the Sync Generator operates and which can be studied in greater detail with the simplified schematic of REFERENCE 4. The third functional area, output sync and blanking, is shown in REFERENCE 2. The top portion, an overview of the simplified schematic of REFERENCE 5, shows the sync generator IC and the sync input signals. The bottom section shows the advanced reference sync generator IC loop for nonservoed capstan VTR's which is given in more detail in REFERENCE 6. The simplified schematics with their associated waveforms (REFERENCE 7) fill in more detail of the sync generator operation only touched on in the discussion that follows.

15-3. Reference Video Sync Processing

EIA standard RS170A expresses the relationship of horizontal sync to subcarrier as the zero crossing of subcarrier relative to the leading edge of horizontal sync. This is equivalent to considering the subcarrier as the reference, and that the leading edge of horizontal sync is coincident with a zero crossing of subcarrier. Because the horizontal line contains 227-1/2 cycles of subcarrier, the phase of the leading edge of horizontal sync relative to subcarrier changes by 180 degrees (140 ns) on alternate lines. The subcarrier does not shift in phase (relative to itself) from one line to the next; nor does the sync pulse shift. Because subcarrier frequency is an odd multiple of one-half the horizontal rate, the zero crossing coincident with the leading edge of sync will be positive going on one line and negative going on the next. This relationship will continue for each alternate line. (See Figure 15-1, Color Field Phase Relationships.)

The phase relationship of vertical sync relative to subcarrier, and color frame relative to carrier is much more subtle. As noted above, the phase of H-sync to subcarrier changes on alternate lines. Each field contains 262-1/2 lines (50,718.75 cycles of subcarrier). Each frame contains 525 lines (119,437.5 cycles of subcarrier). Since the frame ends on a one-half cycle, it can be seen that the phase of the vertical rate relative to subcarrier will change by 180 degrees each alternate frame. (See Figure 15-2, Frame 7.8-kHz Phase Correction Circuit Timing Diagram.)

The phase relationship of 7.8-kHz (as it is used in the TBC) to horizontal sync changes at the transition between each even-numbered field and the following odd-numbered field of the color frame, between frame A and frame B of the color field, and between field 4 and field 1 of the following color frame.

15-4. Burst Crossing (See REFERENCE 3.) Since horizontal sync changes phase by 180 degrees (140 ns) relative to subcarrier on alternate lines, the frame 7.8 kHz shifts burst-crossing enable by 140 ns on each alternate line. This insures that the selected burst crossing is always detected at the zero crossing on a positive-going transition. If the frame 7.8 kHz comes up in an incorrect phase of startup, a circuit consisting of U34-5 and U35-6 will reclock the frame 7.8-kHz flip-flop to the correct phase and will be inactive thereafter. Once the correct phase is established, the 7.8-kHz flip-flop will be clocked by delayed H from U49-6. (See Figure 15-2, Frame 7.8-kHz Phase Correction Circuit, Timing Diagram.)

15-5. Frame Lock. See REFERENCE 3 and Waveform Series A–D and M–Q. Frame-lock circuitry provides a third phase-locked loop to complete the synchronization of the composite video signal. The vertical broad pulse detector circuit uses the characteristics of the difference between the vertical blanking interval signals of field 1 and field 2 of the video frame to identify field 2. The broad pulse gate (waveform 26) identifies the third serration of the vertical sync signal. The 2 X H rate suppressor permits only the horizontal sync pulses to pass. The H-sync for line 5 of the vertical blanking interval is only coincident with the third serration in field 1 and field 3 of the color frame. The three signals, 2 X H rate suppressor, 3rd broad pulse gate, and 7.8 kHz are AND'ed to produce the color frame pulse (see Waveform 27) to the vertical reset counter and the frame rate reset circuit.

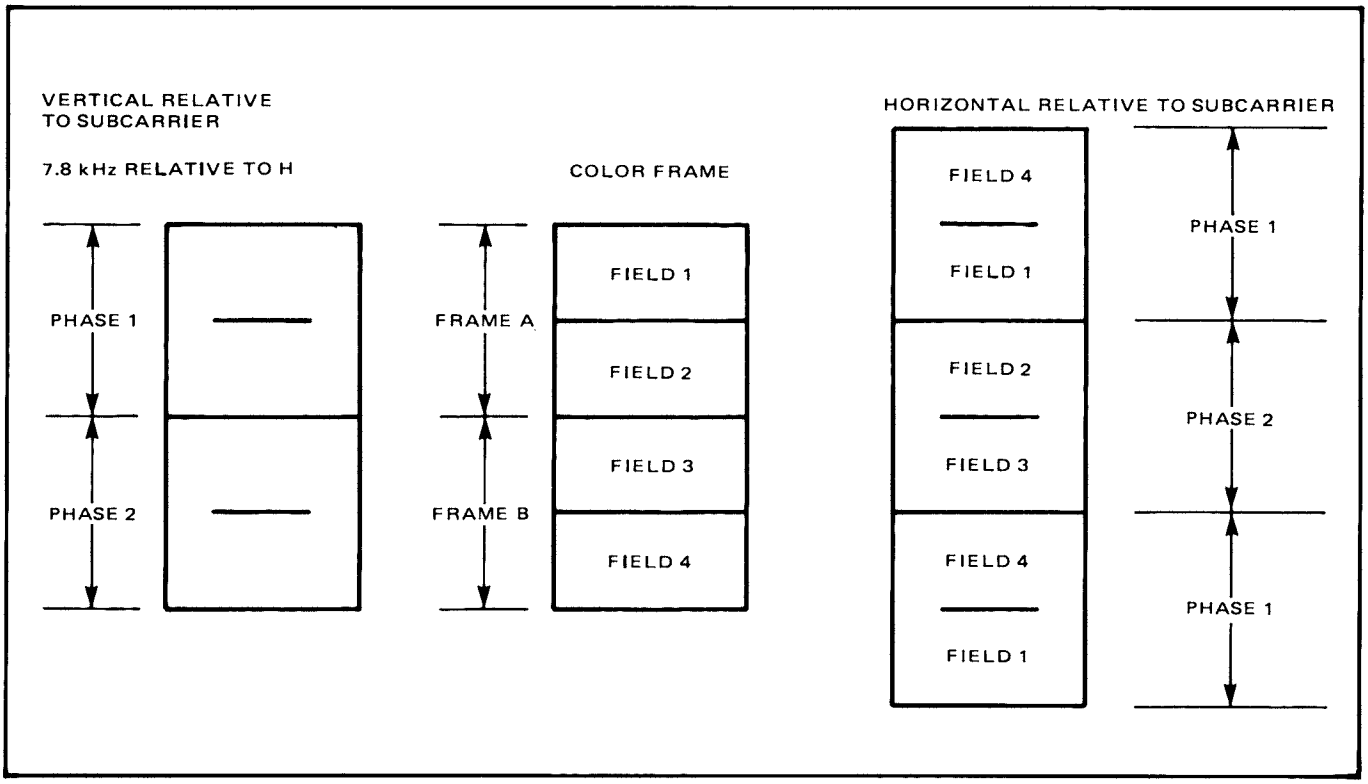


Figure 15-1. Color Field Phase Relationships

As illustrated in Figure 15-1, Color Field Phase Relationships, the frame 7.8-kHz signal changes phase relative to horizontal sync at the transition between frame A and frame B of the color frame. Therefore, the color frame reset pulse represents either the first or third field of the color frame depending on the condition of the flip-flop at startup.

The first equalizing pulse of the first and third fields of the color frame is coincident with the horizontal sync of line 1 of the field. This is not true of the second and fourth fields. The equalizing pulse detector takes advantage of this condition to produce a pulse at the start of field 1 and of field 3. The pulse from the frame detector (field 2 or 4) sets the frame rate reset flip-flop. The pulse from the equalizing pulse detector clocks the flip-flop. The result will be a color frame rate reset 15-Hz pulse to the reference 3.58-MHz quad phase circuit and the reference 7.8-kHz circuit, thereby locking the reference output synchronizing signals to the color frame. It should be noted that the 14.3-MHz oscillator which is phase-locked (gen-lock) to the station master H-rate, clocks the reference 3.58-MHz divide-by-four circuit. One phase of the 3.58-MHz signal reclocks the H-drive from the sync generator integrated circuit to the horizontal phase comparator. The 14.3-MHz oscillator, which is normally phase-locked to station master burst crossing, provides a 2-MHz clock via the divide-by-seven counter to the sync generator integrated circuit. The sync generator integrated circuit provides the output synchronizing signals which are a part of the various feedback loops of the Sync Generator PWA. Therefore the outputs of the Sync Generator PWA are firmly locked to all components of the station reference video.

15-6. Vertical Blanking and Reset Counters. (See REFERENCE 3.) The broad pulse gate from U43-7 provides a high to the D-input of U53-2. The line 5 H-pulse clocks it through to clear the vertical blanking counter U63 to zero. The counter is clocked by H-rate pulses from U34-13. When the Q_D output of U63 goes low on count 256, one-shot U62 is triggered at the beginning of the vertical blanking interval time. This signal inhibits

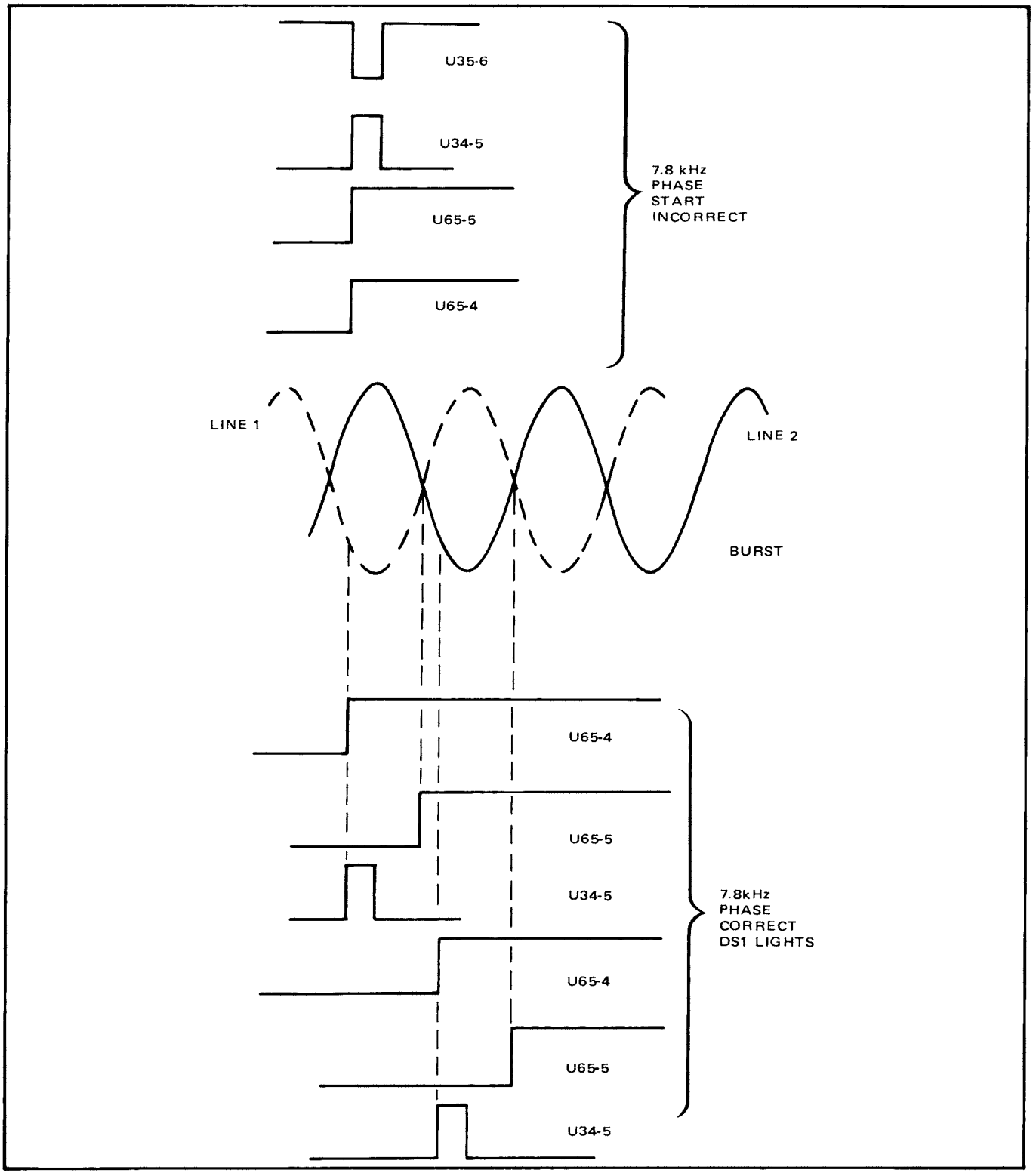


Figure 15-2. Frame 7.8-kHz Phase Correction Circuitry, Timing Diagram

the horizontal phase comparator, the burst present and burst crossing detectors, and the gen-locked indicator during the vertical blanking interval. The 14.3-MHz oscillator must, therefore, free-wheel for approximately 22 lines.

The vertical reset counter (U45, U56, U55) is a 12-bit binary counter capable of counting 4,096 clock pulses if started at a count of zero. To achieve the desired counts of less than this amount, some of the programmable inputs are hard-wired either high or low. Other inputs are programmed by signals from the VTR. The programmed number is loaded when the color frame rate pulse pulls the load inputs low. The H-rate pulse clocks the counter until the carry output resets the sync generator integrated circuit. The counter will roll over to zero and continue to count, but will be reset four frames later before another carry can be generated. In the normal condition, vertical reset will occur five horizontal lines less than one complete field after the start of the count. The color frame rate pulse occurs five and one-half to six lines into the vertical interval. With a minus-five line count, sync generator IC will be reset at the beginning of the vertical blanking interval once during the color field. The zero offset signal from the VTR is used in E–E operation, or direct electronic transfer of signal. When zero offset is low (active) the count will be 263 H-pulses or one complete field. When sync retard is low (active) the VTR is in edit mode, recording video and reading video 120 degrees (approximately one and one-third fields) later on the read head. The one and one-third field plus 6-H count for the vertical reset signal compensates for the one-third field delay of the read head.

15-7. Basic Phase Comparator Loop

Follow the basic loop through REFERENCES 4 and 5. The heart of the Sync Generator PWA is the MM5321N large scale integration (LSI) sync generator and the phase-locked loop (gen-lock) necessary to lock the LSI circuit to the station master reference video in. The loop contains two oscillator circuits; one is crystal-controlled and is used for color video with servoed capstan VTR's, the other is an LC circuit and is used with non-servoed capstan VTR's and/or with monochrome video. If burst is not detected for more than approximately 12 lines, the LC oscillator will be automatically switched in. In the case of a non-servoed capstan VTR, the reference control switch on the Video Processor PWA 16 must be changed to VERTICAL.

The reference time base for control and sync signals produced by the Sync Generator PWA is established by either of two 14.3-MHz oscillators; one is crystal controlled and the other is an LC circuit. The crystal oscillator is used when the TBC is allied to a servoed capstan VTR such as the Ampex VPR series. When turned to the VERTICAL position, the reference control switch on the Video Processor PWA 16 replaces the crystal oscillator with the LC oscillator as the central timing circuit of the Sync Generator PWA. The LC oscillator is used when the TBC is allied to a nonservoed capstan VTR. In this mode of operation, time-base errors continue to be corrected on a line-by-line basis, but the vertical rate time-base errors are preserved because the 14.3-MHz LC oscillator is slaved to the vertical rate time-base error. If the resulting video is recorded on a servoed capstan VTR, passed through the TBC a second time, and re-recorded on a servoed capstan VTR, the final tape will be fully time-base corrected.

The H-drive output of the Sync Generator PWA integrated circuit is applied to one input of a horizontal phase comparator. The other input is referenced to a selected H-sync. For color video, a selected burst crossing is used. For monochrome operation, reference H-sync is selected. The resulting error voltage is applied to the 14.3-MHz oscillator circuit. The phase-corrected 14.3 MHz is applied to a divide-by-seven counter and a divide-by-four counter. The divide-by-seven counter generates a 2-MHz clock as the basic reference for the Sync Generator integrated circuit. The divide-by-four counter produces a 3.58-MHz signal. The Sync Generator integrated circuit requires a vertical reset input in order to provide composite sync that is slaved to the reference video in.

15-8. Advanced Reference

See REFERENCE 6 and Waveforms 10 and 22. A second MM5321N sync generator integrated circuit generates a VTR-advanced reference signal

to provide a 5-1/2-line advance of off-tape video from the VTR with respect to the read function of the TBC-2 Memory PWA's. The Ampex VPR-2 generates its own advance and does not use this signal. The vertical drive signal from the first sync generator integrated circuit is phase-compared with the tape vertical signal from the Tape VCO PWA 6. The resultant error voltage provides a servoed advanced vertical reset to the second sync generator integrated circuit. If a non-servoed capstan VTR is used, the same error voltage will be applied to the LC 14.3-MHz oscillator. If the TBC-2 is used with a VTR which cannot accept a servoed 5-1/2-line advance, a fixed 5-1/2-line advance may be accessed by a jumper on the Sync Generator PWA.

15-9. SYNC GENERATOR MAINTENANCE

See REFERENCE 8 and REFERENCE 9 in this section for the component locator diagram, jumper/test-point/adjustable-component summaries, and waveforms called out in these procedures.

Before undertaking any adjustments to the Sync Generator PWA review the *System Alignment Guide* (Table 3-2) and the *Tape/Reference Test Loop* discussion (Paragraph 3-5) in the *System Maintenance* section (Part I) for a general understanding of the scope of these field adjustments.

Consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the interactive functions between the Sync Generator and interactive functions between it and other PWA's before making any adjustments. For example, some of the adjustments here require a normal signal from the Video Output PWA.

15-10. SYNC GENERATOR ALIGNMENT

The Sync Generator PWA is set at the factory for operation with reference video which conforms to the RS170A standard for burst-to-H sync phasing. This procedure may be used to return the TBC to the original RS170A standard or to re-align the sync generator to a nonstandard reference. Using a nonstandard reference may require adjustment of the PWA 5 Tape H burst/sync phase (R1) to nonstandard for properly color-framed tape interchange. It may also be necessary to perform the *Tape H Sync (Write) Timing* (Paragraph 3-13) given in the *System-Level Maintenance* section.

Whatever burst/sync phase is used, it must be maintained throughout the Sync Generator PWA alignment.

15-11. Input Sync and Chroma Processing

15-12. Initial Setup.

1. Use the basic tape/reference test loop setup with a color-bar signal at standard level to TAPE VIDEO IN. The waveform monitor and vectorscope will be used later in the procedure.
2. With power off extend the Sync Generator.
3. Turn power on and verify that control panel GEN LOCKED indicator is on.

15-13. Burst and Chroma Filters.

1. Connect oscilloscope:

   Channel 1: TP 1 (filtered video, nominal 5 Vp-p)

   Trigger: Internal

2. Adjust L1 (video low-pass filter) for minimum subcarrier on steps.
3. Verify TTL-level composite sync at TP3.
4. Verify a 0.25 (± 10%) Vp-p chroma level and a 0.475 (± 10%) Vp-p burst level at TP2.

15-14. Burst Crossing Selector.

1. Connect oscilloscope:

   Channel 1: TP11 (reference video)

   Channel 2: TP12 (comparator reference burst)

   Trigger: TP3 (composite sync)

2. Verify that the pulse on channel 2 (TP12, approximately 300 ns) occurs near the center of the burst (TP11). See WF1/WF5(B).

3. Connect oscilloscope:

   Channel 1: TP13 (delayed reference sync)

   Channel 2: TP12 (comparator reference burst)

   Trigger: Signal Generator H drive

   It is crucial to display the double pulse as shown in WF34/WF35(V). Use oscilloscope delayed sweep and chop mode.

4. Adjust R225 (alternate line 140 ns) for 140 nanoseconds between the positive edges of the two pulses on channel 2 (TP12).

5. Adjust R223 (reference sync/burst calibration) for the center of the second pulse on channel 2 (TP12) to occur at the leading edge of the pulse on channel 1 (TP13). See WF34/WF35(V).

6. Verify that indicator DS1 (reference sync/burst-PWA edge) is on. Note that DS1 will come on at more than one point as R223 is adjusted. For normal color framing the indicator must be on as indicated above for the odd field burst crossing. If the indicator is not on the sync generator may alternately select any burst crossing making read timing unstable.

7. Verify the following signals:

   a. TP7 (reference burst) – H rate, nominal 400 ns width.

   b. TP6 (14.3 MHz) – see WF13(G).

15-15. Color/Mono Lock.

1. Connect oscilloscope:

   Channel 1: TP15 (crystal oscillator error)

   Trigger: Line

2. Adjusts L9 (crystal oscillator frequency) for 0 Vdc.

3. Verify that error voltage at TP15 shifts and then returns to 0 Vdc for each of the following conditions:

   a. Switch power off and on.

   b. Switch TAPE/NORMAL (Video Processor PWA 16 edge) to TAPE then NORMAL. This is part of an option; grounding PWA 15 Pin 26 will accomplish the same thing.

   c. At signal generator turn burst off and on.

   d. Disconnect and reconnect reference video at input.

   Repeat as required to insure proper lock.

4. Connect oscilloscope:

   Channel 1: TP14 (LC oscillator error)

   Trigger: Line

5. Switch burst off at the signal generator.

6. Adjust L3 (LC oscillator frequency) for 0 Vdc.

7. Verify that error voltage at TP14 responds oppositely to conditions a, b, c, and d in step 3 above.

15-16. Preliminary Sync and Chroma Timing

1. Return burst to the input video.

2. Connect oscilloscope:

   Channel 1: TP8 (reference 3.58 MHz)

   Trigger: Internal

3. Adjust R173 (chroma symmetry) for a symmetrical square wave. See WF16(I). Because this signal is terminated it is below normal TTL level.

4. Connect oscilloscope:

   Channel 1: TP9 (subcarrier)

   Trigger: Internal

5. Adjust R226 (subcarrier symmetry), L7, and L8 (subcarrier filter) for peak output of the 3.58-MHz sine wave. See WF17(I).

6. Verify a symmetrical 7.8-kHz square wave at U21-10.

15-17. Color Frame Detector. Do not adjust R70 (third broad pulse detector level) until the four fields and the position of the frame pulse are clearly identified in the context of the procedure and need for adjustment is definitely established. Make certain also that burst crossing is properly calibrated and the reference sync/burst indicator is on.

1. Connect oscilloscope:

   Channel 1: U43-7 (broad pulse gate)

   Channel 2: U43-2 (integrator)

   Trigger: PWA Pin 69 (or signal generator V drive)

2. Using delayed sweep, scan four fields of video. The positive edge of the pulse on channel 1 should be coincident with center of the third (from the bottom) transition on the ramp on channel 2 for the odd field. The normal condition is shown in WF25/WF26(P). If the channel 1 pulse occurs anywhere on the third transition do not adjust R70 but proceed to the next step.

3. Connect oscilloscope:

   Channel 1: TP11 (reference video input)

   Channel 2: U52-8 (color frame pulse)

   Trigger: PWA Pin 69

4. The desired display is shown in WF27(Q). Use delayed sweep and scan at least four fields. The color frame pulse is difficult to see and should occur on only one of the four fields.

5. If the color frame pulse is at the vertical third broad pulse, do not adjust R70; it will jump to the fourth broad pulse of the even field. If the frame pulse is coincident with the fourth broad pulse adjust R70 for coincidence on the third broad pulse. Re-check ramp coincidence of step 2.

6. As a further check on the validity of the adjustment compare reference video against TBC video out and note field-for-field coincidence of vertical interval sync pulses.

15-18. Output Sync and Blanking

15-19. Initial Setup. Continue the setup of the first part of this Sync Generator PWA procedure but select a color black signal at the generator and leave PWA in its slot for adjustment of blanking controls on the PWA edge.

15-20. Horizontal Blanking. H-blanking leading/trailing edges may be set at any time to the user's requirement but should be checked at this stage to insure that any misadjustment of the edges does not interfere with burst adjustments in the next part of the procedure.

1. Connect oscilloscope or waveform monitor to VIDEO OUT 1 and display horizontal interval.

2. Pull out BLACK LEVEL control and turn it fully clockwise to observe pedestal.

3. With reference to the H-interval illustration in the proposed RS170A standard (Figure 2-n in Part I) adjust R46 (H-blanking leading edge) for a horizontal front porch between 1.0 and 1.2 microseconds.

NOTE

This is not RS170A standard. A very wide leading edge established here may interfere with rise-time adjustments of L4, L5, and R65 on the Video Output PWA. Most users keep the blanking narrower than RS170A standard to avoid losing picture video in the many production steps and to avoid contributing to a widening of the sync interval of the broadcast signal.

4. Adjust R45 (H-blanking trailing edge) for an interval (sync leading edge to blanking end) between 9.5 and 9.9 microseconds.

5. Verify that the 50% point of the first cycle burst lags the negative edge of H-sync between 5.2 and 5.4 microseconds.

15-21. Vertical Blanking. Normal speed vertical blanking is set for the user's requirement and the trailing edge may be set as far down as line 10 to unblank any vertical interval test and control signals. It is usually set for blanking of the line preceding such signals and may also be set as high as line 25 to blank out signals in lines 1-25. In slow-motion operation, test and control signals are blanked out (to prevent interference by the irregular field repetition of the slow-motion process).

Adjustment may be made with the basic tape/reference test loop or during tape playback with the VTR. In either case, slow-motion control of the VTR will be used for the R65 (slow-motion vertical blanking) adjustment.

1. Connect oscilloscope or waveform monitor to VIDEO OUT 1 and display vertical interval.

2. Pull out BLACK LEVEL control and turn it fully clockwise.

3. With a VITS on line 16 (or user's preferred VITS line position) and the input to the TBC, adjust R64 (normal V-blanking) so that the first line after the equalizing pulses (line 10) is the first unblanked line.

NOTE

Unblanked lines will show a pedestal, blanked lines will not.

4. Switch to slow motion at the VTR.

5. Adjust R65 so that the line with the VITS signal is blanked out through its pedestal.

NOTE

Adjustment of R65 here must be coordinated with the adjustment of R320 (vertical clamp timing) on PWA 14. See Paragraph 14-11, *White Bar Suppression.*

6. Return BLACK LEVEL to unity.

15-22. Advanced Reference Sync

There is no need for adjustment of the advance reference except with a particular heterodyne VTR. Refer to *Heterodyne Operation,* Paragraph 3-18, PART 1, for guidance to operation with heterodyne and nonservoed capstan VTR's.

15-23. Output Subcarrier and Chroma Phasing

1. Continue the tape/reference test loop setup and add waveform monitor and vectorscope for input/output comparison. Use a 75% color-bar signal at standard level and RS170A sync/burst phase (or normal phase of the facility). This procedure assumes normal operation in previous Sync Generator PWA test stages.

2. Verify the following conditions:

   a. Indicator DS1 (reference sync/burst phase calibration) is on.

   b. Reference 3.58 MHz signal at PWA Pin 79 (TP8) is a symmetrical square wave as adjusted by R173 (chroma symmetry).

   c. Subcarrier signal at PWA pin 75 (TP9) is set for maximum level as adjusted by R226 (subcarrier symmetry), L7 and L8 (subcarrier filter).

   d. Quad phases are available at U49-8, -12, -2, and -4 as shown in WF14/WF15(H). The four phases may also be checked by viewing PWA Pin 79 (Reference 3.58 MHz) with the vectorscope (locked to external reference phase) and shifting jumper J4 in the following sequence: B–D, B–E, B–C, and B–A, but be sure to return the jumper to its original position.

3. While observing input/output video signals on waveform monitor (A–B mode), superimpose

H-sync leading edges within a subcarrier cycle with the HORIZ PHASE control on control panel.

4. Observe chroma/burst on the vectorscope (locked on external subcarrier) and adjust SUBCARRIER PHASE on the control panel so that burst vectors are aligned. Bursts seen on waveform monitor will nearly cancel.

NOTE

If bursts cannot be aligned or either HORIZ PHASE or SUBCARRIER PHASE are not near their center positions, an adjustment of PWA edge control R208 (subcarrier phase) will shift the subcarrier phase without affecting H-sync leading edge.

5. Adjust R208 (subcarrier phase) to align burst vectors. If more range is required, reposition jumper J3. Switch power off to change the jumper and to adjust R208 with PWA in the cage.

6. Turn control panel SUBCARRIER PHASE through its range and confirm a shift of 370° as viewed on the vectorscope. If the range is not 370° proceed as follows:

   a. With power off extend the PWA.

   b. Adjust R199 (subcarrier phase range) to achieve a 370° shift of SUBCARRIER PHASE control.

   c. Return PWA to the cage and restore subcarrier phase alignment determined in step 5.

7. Pull CHROMA PHASE control out and center it.

8. Adjust R146 (chroma phase – PWA Edge) so that chroma vectors are aligned on vectorscope. If more range is required, select a new position for J4. Remember to switch power off to change the jumper and to adjust R146 with PWA in cage.

NOTE

If changes to the write timing at the Tape H/Tape VCO PWA's are made subsequent to this test it may be necessary to recheck this step.

9. Verify that for both the control panel CHROMA PHASE and R146 turned simultaneously to either extreme, there is no picture shift. If there is a horizontal shift proceed as follows:

   a. With pwoer off select opposite position (A–B or A–C) for jumper J5.

NOTE

There is no normal position for J5. It is used to insure that the sync generator phasing does not create an unwanted H-drive/subcarrier phase coincidence on the Memory Control PWA.

   b. Re-check CHROMA PHASE/R146 extremes for no horizontal picture shift.

   c. Return PWA to the cage.

10. Restore chroma vector alignment determined in steps 7 and 8.

11. Check control panel CHROMA PHASE range as follows:

   a. Mechanically center the unity chroma phase trim control (control panel top/center).

   b. Push in CHROMA PHASE control.

   c. Adjust vectorscope variable phase control for the yellow vector to be on a convenient reference point on the graticule.

d. Pull out CHROMA PHASE control and note amount of vector swing on either side of reference.

e. Push CHROMA PHASE in.

f. Adjust unity trim control in direction of the largest swing.

g. Re-establish a yellow vector reference.

h. Repeat steps c through g until the vector swings approximately 20° in either direction from reference setting.

12. Return vectorscope to external lock and repeat steps 7 and 8.

13. Push CHROMA PHASE in and adjust unity trim for coincidence of the chroma vectors. This step completes phasing of the TBC to the system reference.

15-24. Output Sync/Burst Phase (Non-RS170A)

As factory calibrated, the Sync Generator PWA inserts sync on corrected video that conforms to proposed standard RS170A for sync/burst phasing. The use of OUTPUT SYNC/BURST control R240 allows matching standard RS170A output to any video source where a displacement of H-sync phase is required without affecting subcarrier phase. This procedure sets up range and symmetry for output sync/burst control, R240. To phase the TBC to the reference source refer to *Non-RS170A REFERENCE PHASING,* Paragraph 3-nn in the *System Maintenance* section.

1. Use the tape/reference test loop with standard level 75% color bars and RS170A burst/sync phase.

2. With power off, extend Sync Generator.

3. Position jumper J6 to B–C.

4. Connect oscilloscope to U74-13; trigger on internal.

5. Adjust R72 (symmetry) for a symmetrical square wave.

6. Connect oscilloscope to U74-12; trigger on internal.

7. Preset R240 fully clockwise.

8. Adjust R245 (range) for a positive 200-nanosecond pulse.

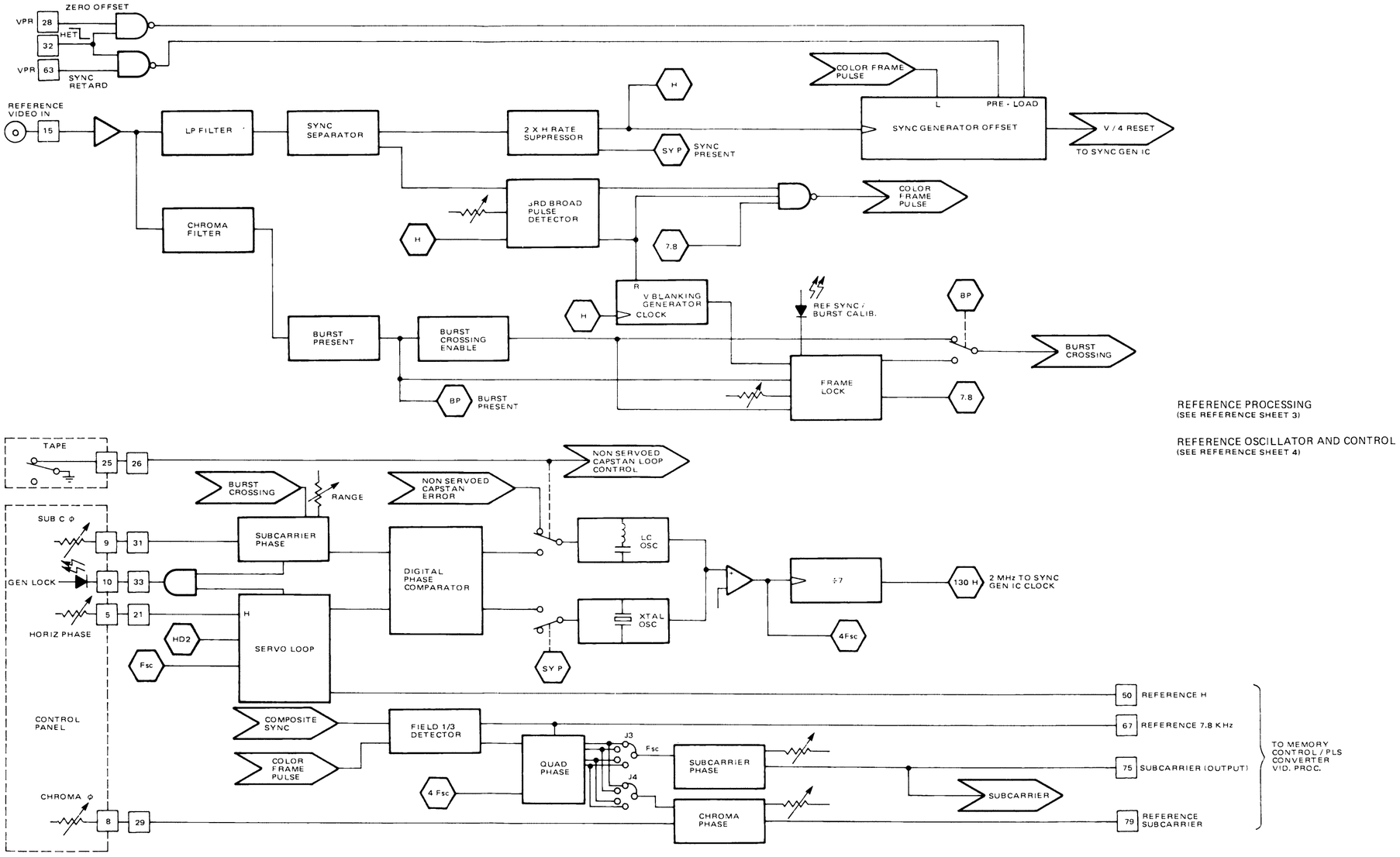
9. Connect oscilloscope to VIDEO OUT 1; trigger on signal generator H-drive output.

10. Use delayed sweep and display leading edge of the H-sync.

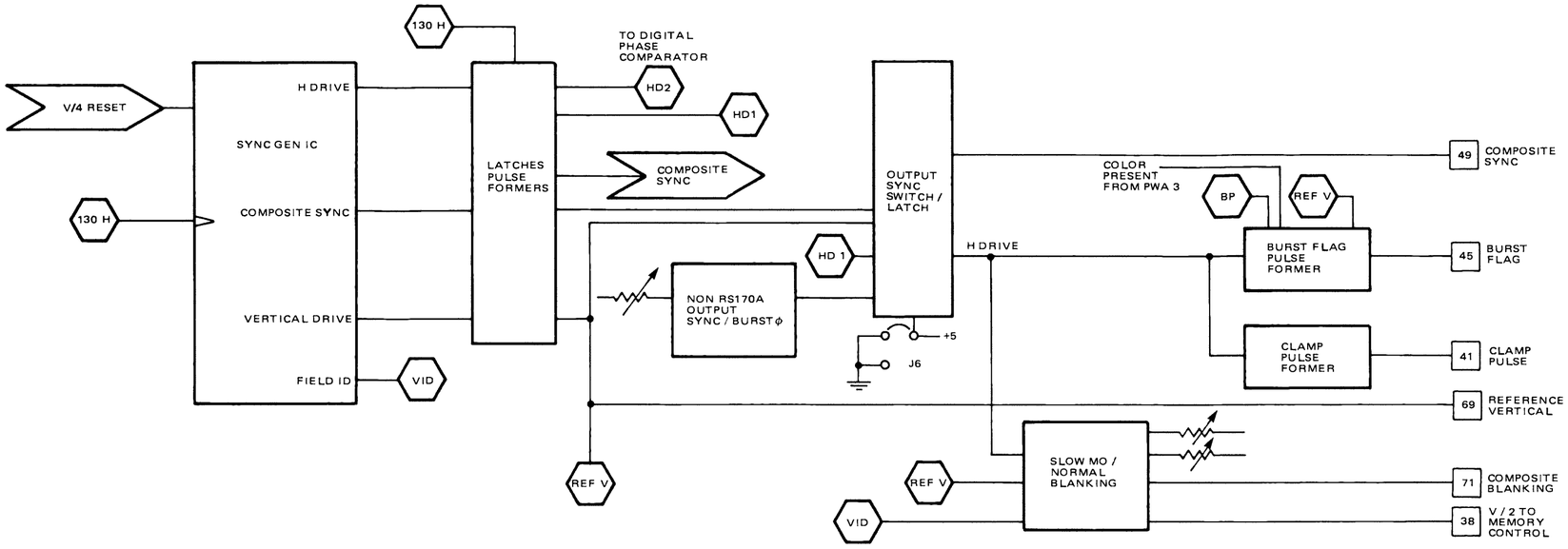
11. Adjust R240 through its range – at least 270 nanoseconds but no more than 300 nanoseconds.

12. Adjust R245 to limit range of R240 to 270–300 nanoseconds.

13. Return J6 to A–B unless the TBC is to be phased to a non-RS170A source as outlined in the *System Maintenance* section, Part I.

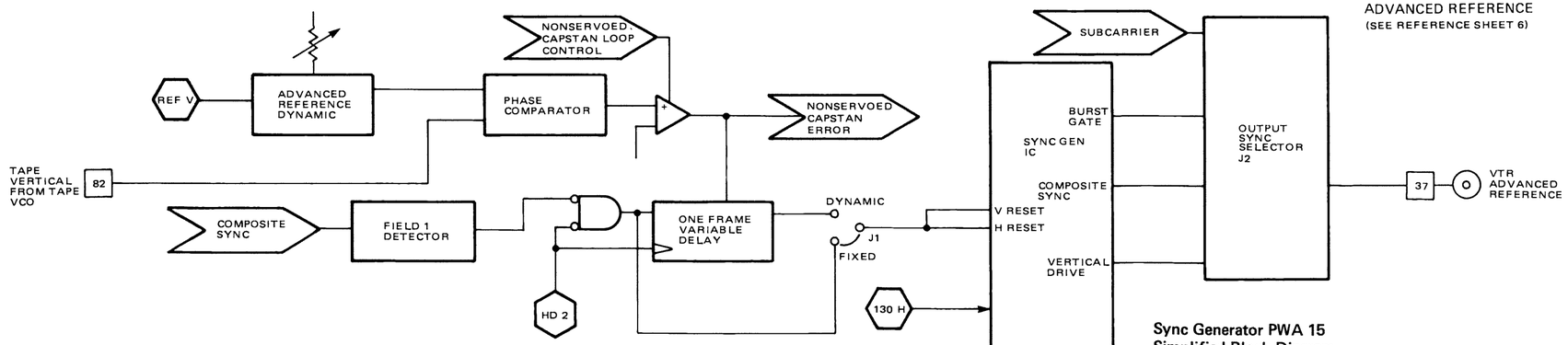


Sync Generator PWA 15
Simplified Block Diagram
REFERENCE 1
(Sheet 1 of 2)

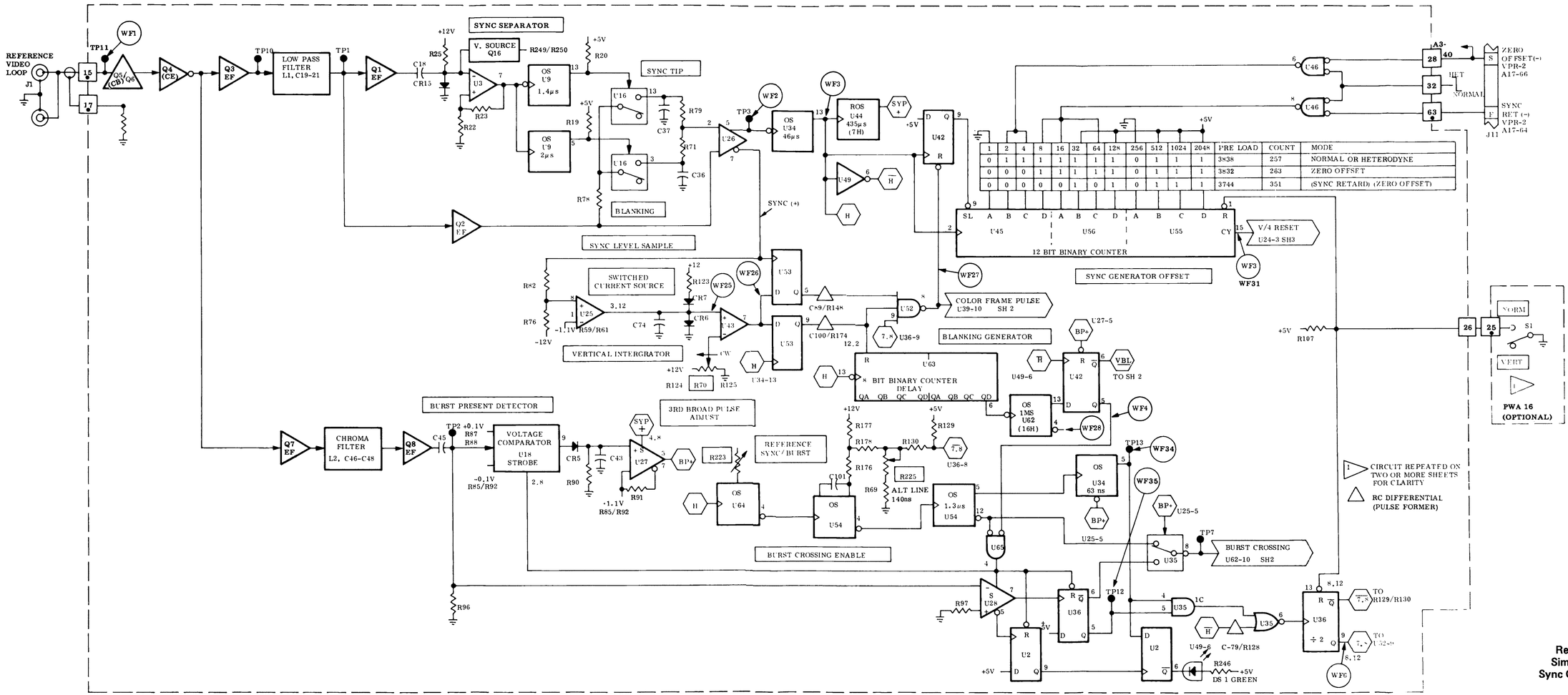


OUTPUT SYNC / BLANKING
(SEE REFERENCE SHEET 5)

ADVANCED REFERENCE
(SEE REFERENCE SHEET 6)



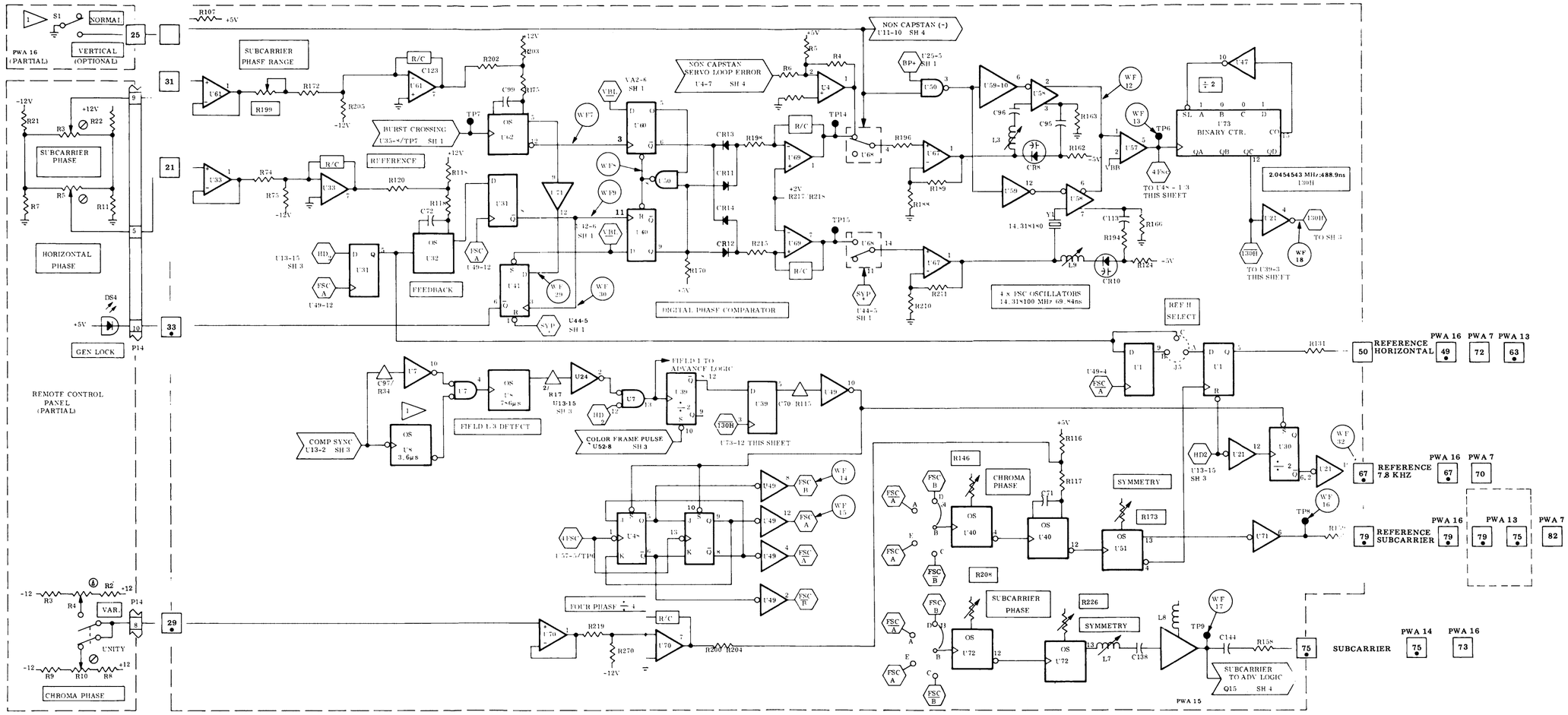
Sync Generator PWA 15
Simplified Block Diagram
REFERENCE 2
(Sheet 2 of 2)



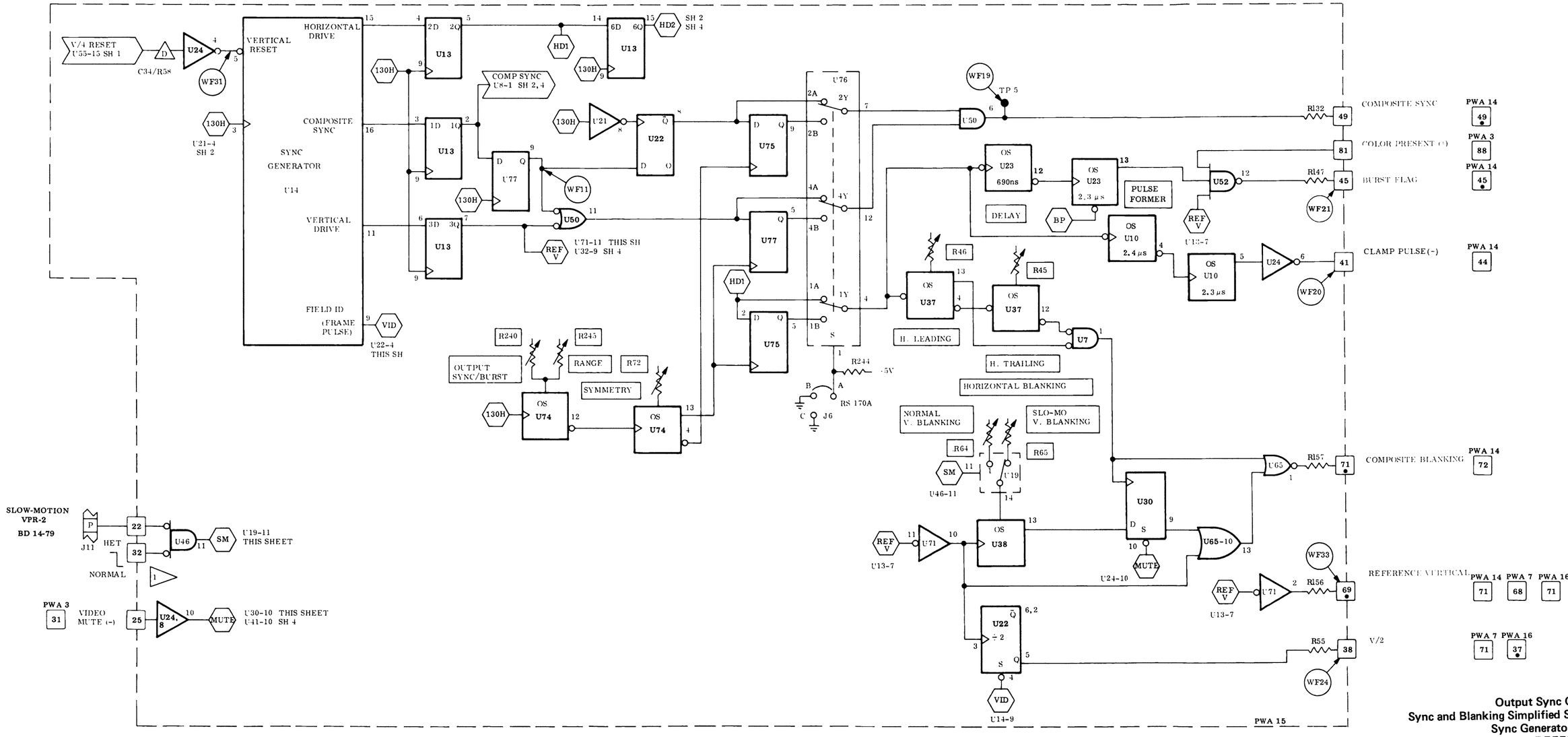
1	2	4	8	16	32	64	128	256	512	1024	2048	PRE LOAD	COUNT	MODE
0	1	1	1	1	1	1	1	0	1	1	1	3838	257	NORMAL OR HETERODYNE
0	0	0	1	1	1	1	1	0	1	1	1	3832	263	ZERO OFFSET
0	0	0	0	0	1	0	1	0	1	1	1	3744	351	(SYNC RETARD) (ZERO OFFSET)

Reference Processing Simplified Schematic, Sync Generator PWA 15 REFERENCE 3

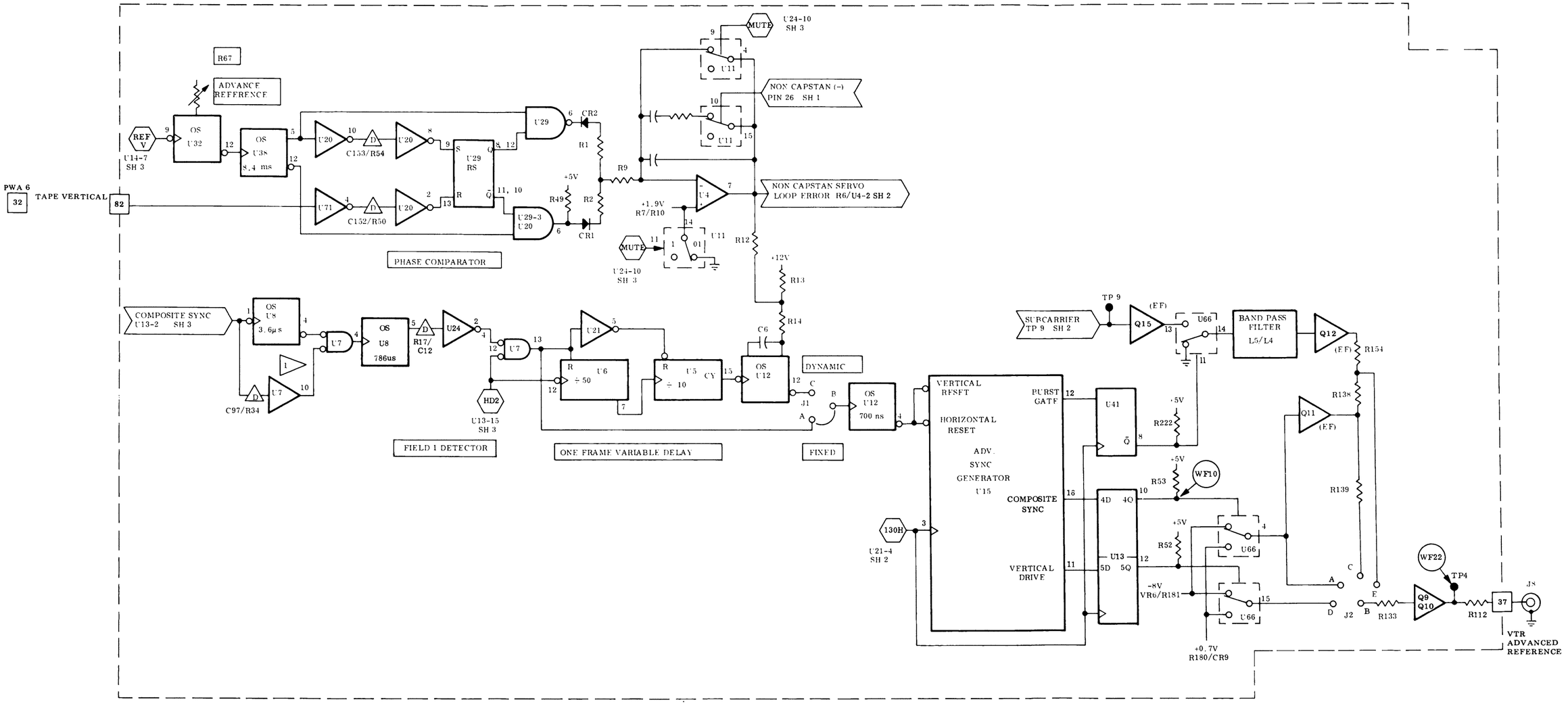
AMPEX 1809474-01



Reference Oscillators Simplified Schematic
Sync Generator PWA 15
REFERENCE 4



Output Sync Generator
Sync and Blanking Simplified Schematic
Sync Generator PWA 15
REFERENCE 5



Nonservoed Capstan Loop
Advanced Reference Simplified Schematic
Sync Generator PWA 15
REFERENCE 6

PART II
15-18

AMPEX 1809474-01

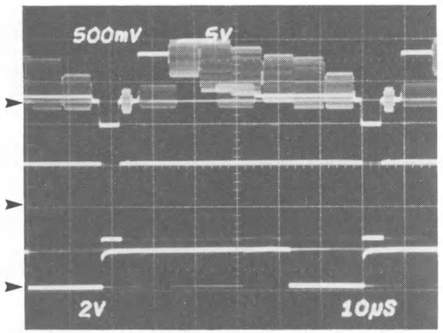
A

TP11
REF VIDEO IN — WF1

TP3 REF
COMPOSITE
SYNC — WF2

U34-13
H RATE
SUPPRESSOR — WF3

TRIG: TP3



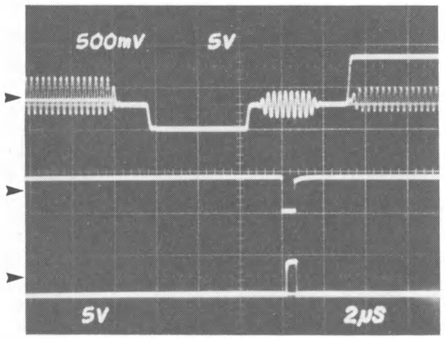
B

TP11
REF VIDEO IN — WF1

U54-12
DELAYED H — WF4

TP12
COMPARATOR
REFERENCE
BURST — WF5

TRIG: U54-12

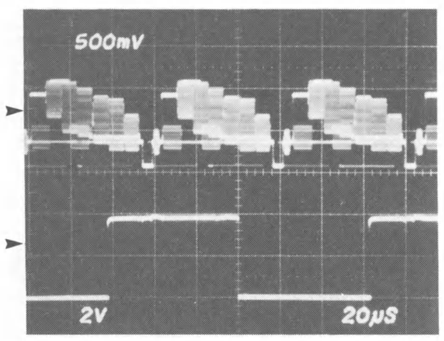


C

TP11
REF VIDEO IN — WF1

U36-9
FRAME 7.8 kHz — WF6

TRIG: U36-9



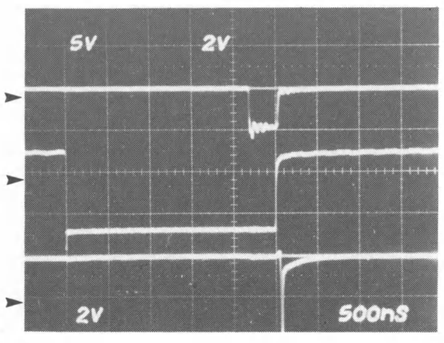
D

U60-3
SELECTED
BURST
CROSSING — WF7

U60-11
DELAYED
H DRIVE — WF9

U50-8
COMPARATOR
RESET — WF8

TRIG: U60-11

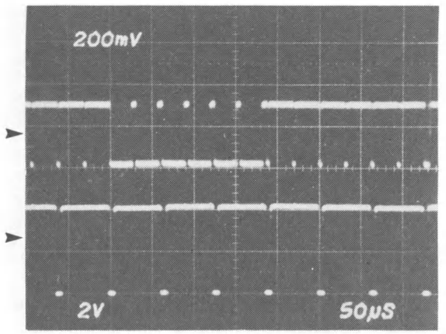


E

TP11
REF VIDEO IN — WF1

U13-15
ADVANCED
COMPOSITE
SYNC — WF10

TRIG: PIN 69
VPR IN PLAY

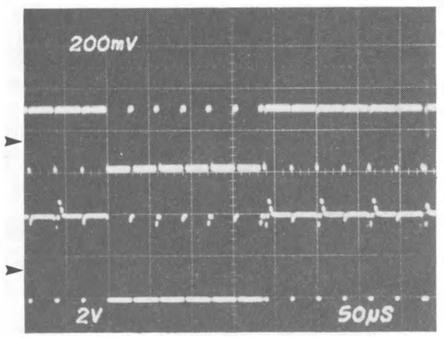


F

TP11
REF VIDEO IN — WF1

PIN 49
OUTPUT
COMPOSITE
SYNC — WF11

TRIG: PIN 69
SCOPE CHOP MODE
VPR IN PLAY

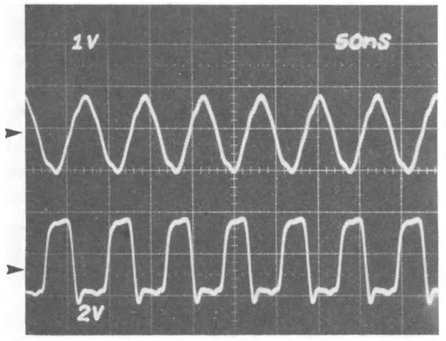


G

U57-1
CRYSTAL
OSCILLATOR — WF12

TP6
SELECTED
OSCILLATOR
OUTPUT — WF13

TRIG: TP6



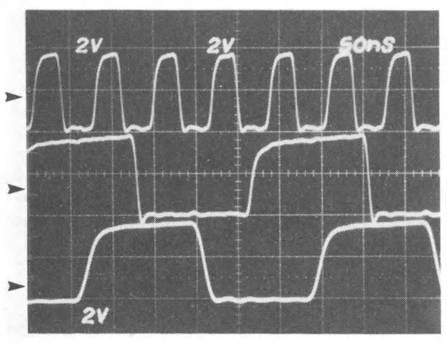
H

TP6
SELECTED
OSCILLATOR
OUTPUT — WF13

U49-8
QUAD PHASE
14.3 MHz ÷4 — WF14

U49-12
QUAD PHASE — WF15

TRIG: TP8



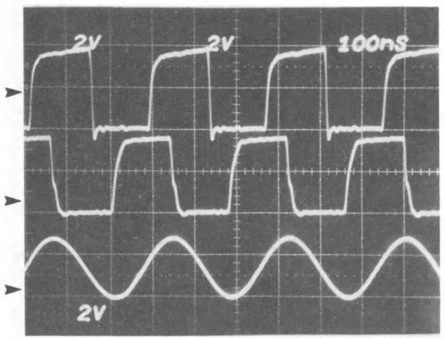
I

U49-8
QUAD PHASE — WF14

TP8
DELAYED
QUAD PHASE — WF16

TP9
SUBCARRIER TO
VIDEO OUTPUT — WF17

TRIG: TP8

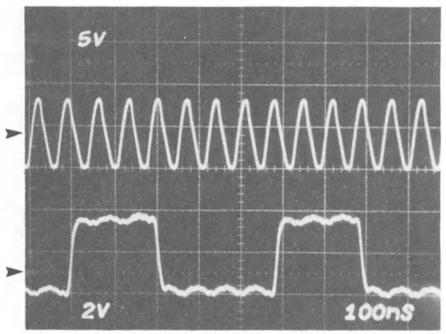


J

TP6
SELECTED
OSCILLATOR
OUTPUT — WF13

U21-4
14.3 MHz ÷7
(130H) — WF18

TRIG: U21-4



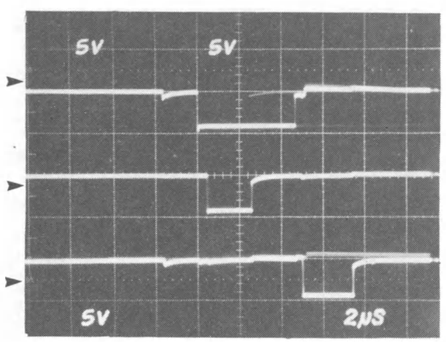
K

TP5
COMPOSITE SYNC
TO VIDEO OUTPUT — WF19

PIN 41
CLAMP PULSE
TO VIDEO OUTPUT — WF20

PIN 45
BURST FLAG TO
VIDEO OUTPUT — WF21

TRIG: PIN 45
VPR IN E/E



Waveforms,
Sync Generator PWA 15
REFERENCE 7

PART II
15-19

L

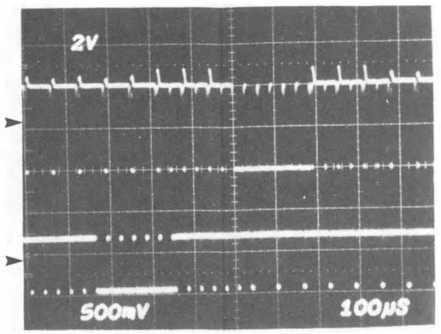
TP5
OUTPUT COMPOSITE
SYNC

WF19

TP4
ADVANCED V
REFERENCE

WF22

TRIG: PIN 69



M

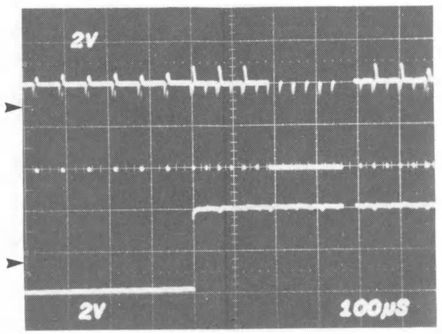
PIN 49
OUTPUT COMPOSITE
SYNC

WF23

PIN 38
V/2

WF24

TRIG: PIN 69



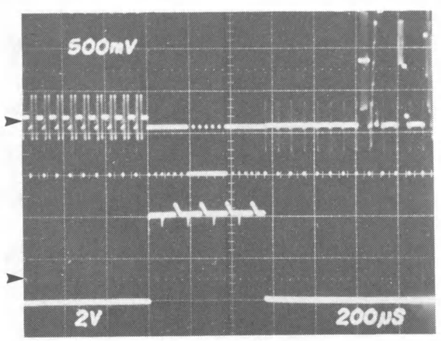
N

TBC VIDEO OUT

WF33

PIN 69
REFERENCE
VERTICAL

TRIG: PIN 69



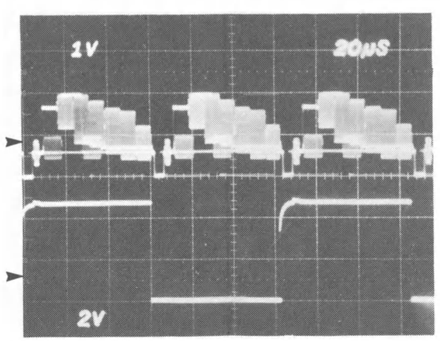
O

TBC VIDEO OUT

WF32

PIN 67
REF 7.8 kHz

TRIG: PIN 67



TP3
REF COMPOSITE
SYNC

U43-2
V INTEGRATOR

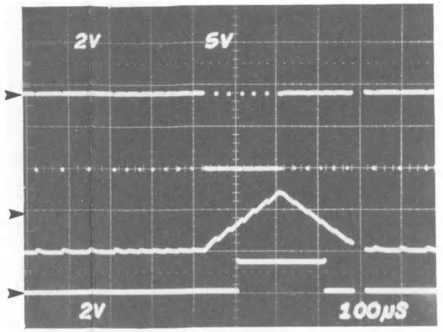
WF25

U43-7
3rd BROAD PULSE
GATE

WF26

TRIG: PIN 69

P



TP3
REF COMPOSITE
SYNC

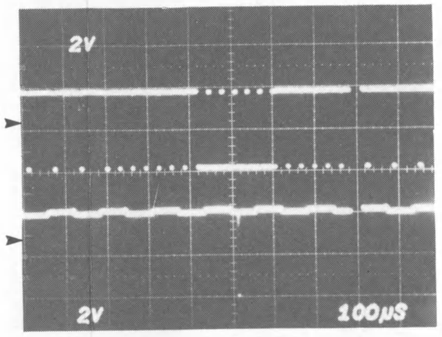
U52-8
FRAME PULSE

TRIG: PIN 69

Q

WF2

WF27



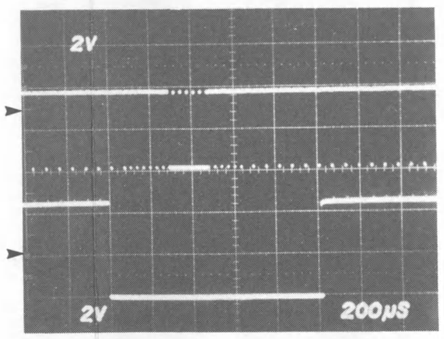
R

WF2

U62-4
V INHIBIT

WF28

TRIG: PIN 69



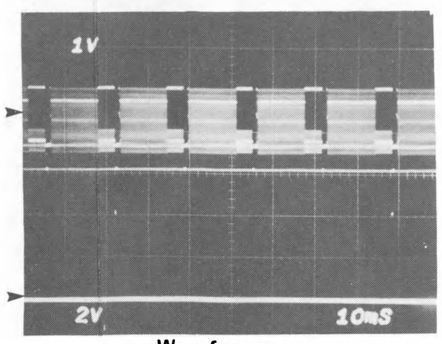
S

TBC VIDEO OUT

U55-15
V/4 RESET

WF31

TRIG: U55-15



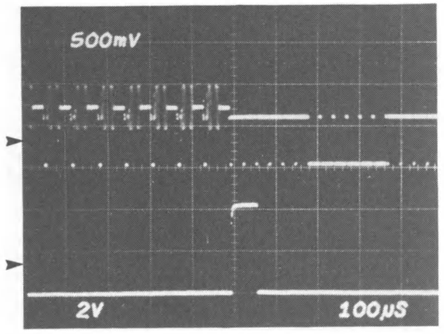
T

TBC VIDEO OUT

U55-15
V/4 RESET

WF31

TRIG: U55-15



U

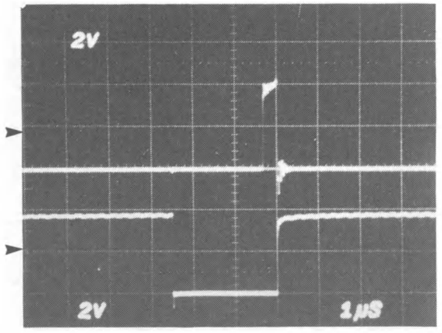
U41-2
SELECTED
BURST CROSSING

WF29

U41-3
DELAYED H DRIVE

WF30

TRIG: U41-3



V

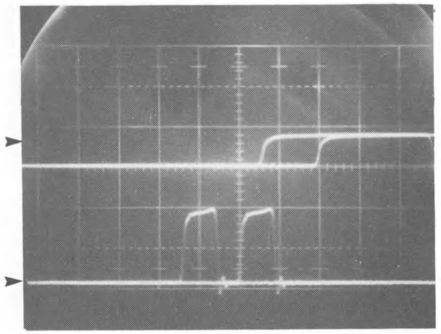
TP13

WF34

TP12
COMPARATOR
REFERENCE
BURST

WF35

TRIG: REF SIGNAL
GENERATOR
H DRIVE



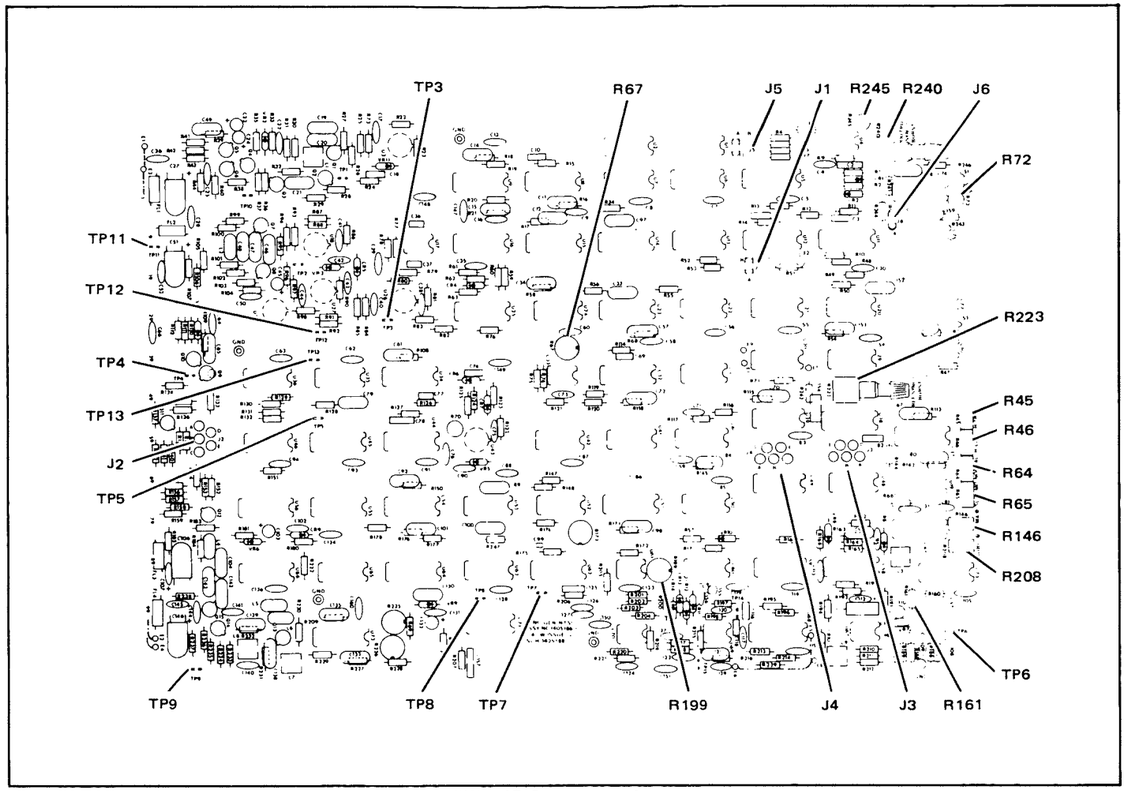
Waveforms,
Sync Generator PWA 15
REFERENCE 8

PWA 15 Jumpers

JUMPER	POSITION – FUNCTION	
J1	A–B	UMATIC Loop 5 1/2 line fixed advance
	B–C	UMATIC Loop servoed advance
J2		Advanced reference output select
	A–B	Composite sync
	B–C	Composite sync (–8V)
	B–D	Vertical (–8V)
	B–E	Sync and burst
J3		Reference 3.58 MHz
	A–B B–C B–D B–E	Select jumper position as required for correct operation
J4		Subcarrier
	A–B B–C B–D B–E	Select jumper position as required for correct system operation
J5		H-phase select
	A–B A–C	Select jumper position as required for correct system operation
J6	A–B	RS-170 standard
	B–C	Nonstandard

PWA 15 Adjustable Components

COMPONENT	FUNCTION
L1	Video low-pass filter
L3	LC oscillator frequency
L7	Subcarrier filter
L8	Subcarrier filter
L9	Crystal oscillator frequency
R45	H-sync leading edge
R46	H-sync trailing edge
R64	V-sync normal
R65	V-sync slow motion
R67	Reference vertical delay
R72	Output sync/burst symmetry
R70	3rd broad pulse detector level
R146	Chroma phase
R173	Chroma symmetry
R199	Subcarrier phase offset
R208	Subcarrier phase
R223	Reference sync/burst calibration
R225	7.8 kHz detector
R226	Subcarrier symmetry
R240	Output sync/burst
R245	Output sync/burst range (coarse)



PWA 15 Component Locator

Table 5-11. Sync Generator PWA 15 Test Points

TEST POINT	NAME
TP1	Filtered video
TP2	Chroma
TP3	Composite sync
TP4	Advanced reference
TP5	Composite sync out
TP6	14.3 MHz
TP7	Reference burst
TP8	Reference 3.58 MHz
TP9	Subcarrier
TP10	Amplified video
TP11	Video input
TP12	Comparator reference burst
TP13	Delayed reference sync/burst
TP14	LC oscillator error
TP15	Crystal oscillator error

SECTION 16

VIDEO PROCESSOR
DESCRIPTION AND MAINTENANCE

16-1. INTRODUCTION

Refer to the following documents in the *Parts Lists and Schematics* manual:

ASSEMBLY No. 1405146

SCHEMATIC No. 1405170

Numbered data sheets (REFERENCE 1, 2, 3 . . . *n*) to which PWA descriptions and maintenance procedures refer are located at the end of this section as follows:

Overall Block Diagram – REFERENCE 1

Simplified Schematic – REFERENCE 2

Maintenance Data – REFERENCE 3

16-2. DESCRIPTION

When the Video Processor PWA 16 (optional) is installed, the TBC can be used with non-segmented helical scan VTR's that are not capstan-servoed. Playback video from the nonservoed capstan VTR is processed in the TBC, and using a servoed-capstan VTR, is dubbed onto a tape. When the dub is played back on the servoed-capstan VTR and again processed through the TBC, the signal is of broadcast quality. During the dubbing process, the Video Processor PWA enables the operator to observe playback video from the nonservoed capstan VTR on a color monitor.

During the dubbing process the TBC sync generator is locked to the average of the off-tape vertical sync and the TBC removes fast or short-term time-base errors. Burst and sync pulses produced by the TBC sync generator are inserted into the TBC video produced at the Video Output PWA; this video and burst is dubbed onto the servoed-capstan machine. Video and burst are also provided to the Video Processor PWA where they are processed into monitorable color available at the MONITOR VIDEO OUT connector on the TBC connector panel. During playback of the dub, the TBC sync generator is locked to the off-tape horizontal sync, and fully time-base-corrected video is available at VIDEO OUT connectors 1 and 2 on the rear connector panel.

Color from a non-servoed capstan VTR is not normally monitorable on a color monitor due to excessive time-base jitter introduced by the VTR. Reference oscillators in the monitors are normally sluggish and cannot follow rapid phase changes in the burst caused by time-base jittering. As a result, the chroma component of the off-tape video from the non-servoed capstan VTR that is fed directly to a monitor is demodulated with respect to the phase of the monitor's reference oscillator rather than with respect to the phase of the burst with which it was recorded. This results in incorrect and unstable color appearing on the monitor screen. The TBC with a Video Processor PWA enables the monitor to produce acceptable color rendition by providing it with video having relatively stable burst (disassociated from line-to-line jitter) and a corrected burst-to-chroma phase relationship. The Sync Generator PWA, which is locked to vertical sync, provides relatively stable burst. The buffering effect of the TBC provides the line-to-line stabilized chroma. Slower-occurring chroma phase errors due to jittering in the vertical rate are corrected by the Video Processor PWA.

The TBC's video output during the dubbing process contains chroma phase errors due to variation in average off-tape vertical rate. This would appear as hue shifts from frame to frame if applied directly to a monitor. The video processor corrects this by demodulating the chroma to the correct B–Y

and R–Y vectors and then remodulating them on a 3.58-MHz carrier produced by a crystal-controlled oscillator. This crystal-stabilized chroma is sent to the monitor which demodulates it to the correct colors.

To demodulate chroma to its correct B–Y and R–Y components, the video processor makes use of the fact that chrominance and burst are coherent at the TBC's output. Both chroma and burst contain the same time-base errors. This coherence is a result of the fact that the burst is produced by the sync generator which tracks on the average of the off-tape vertical sync and thus varies with jitter (although more sluggishly) in the same way as does the off-tape chroma. The burst is used to control a tunable 3.58-MHz reference generator which also tracks time-base errors and is used to demodulate chroma to the correct B–Y and R–Y components. The errors are cancelled in the demodulation process.

The video processor receives TBC video, separates chrominance from luminance, demodulates chrominance with the signal produced by the tunable reference generator, remodulates chrominance using a crystal-controlled reference oscillator to produce corrected chrominance, and then adds chrominance to luminance.

Incoming video is separated into its luminance and chrominance components by the luminance low-pass filter and the chroma bandpass filter, respectively. Chrominance is demodulated into the B–Y and R–Y components in the B–Y and R–Y decoders. The decode carrier for the B–Y and R–Y demodulation is produced by the decode carrier generator.

The reference subcarrier produced by the sync generator is passed through a phase-adjusting circuit and a ringer in the decode generator and becomes the decoding signal for the R–Y and B–Y components of the chrominance. This decoding signal is passed through a –45° shift circuit before being applied to the B–Y decoder and is passed through a +45° shift circuit before being applied to the R–Y decoder. This produces the necessary 90° phase shift between the B–Y and R–Y decode signals. In order to minimize phase drift of the decoding signal, the decode phase control circuit samples the output of the R–Y decoding circuit during burst time and uses the voltage level sample to adjust the phase of the decoding signal. The phase of the decoding signal is adjusted for maximum amplitude of the R–Y decoder during burst time. The burst sample timing pulse is generated by the sync logic circuit from the reference H-drive signal produced by the Sync Generator PWA. The sync logic circuit also produces sync sampling pulses that are applied to B–Y and R–Y decoders. This pulse is used by the decoders to sample and clamp their outputs during sync time.

B–Y and R–Y encoders remodulate B–Y and R–Y on a crystal-controlled 3.58-MHz carrier. The B–Y and R–Y components are summed together to form crystal-stabilized chroma and then reintroduced into the luminance. The reconstituted video is then passed through a low-pass filter and an output amplifier. A clamp circuit establishes the blanking level of the output video.

Switch S1 routes processed video out of the PWA when the switch is set to TAPE. The TAPE position of S1 also locks the sync generator to the average of off-tape vertical sync. When the switch is set to NORM, output video from the TBC bypasses the video processor.

16-3. VIDEO PROCESSOR MAINTENANCE

See REFERENCE 3 in this section for component locator diagram and jumper/test point/adjustable component summaries.

Before undertaking any adjustments to the Video Processor PWA review the *System Alignment Guide* (Table 3-2) and the *Tape/Reference Test Loop* discussion (paragraph 3-5) in the *System Maintenance* section (Part I) for a general understanding of the scope of these field adjustments.

Consult interconnect data on the simplified schematics to confirm normal operation of the Video Processor PWA and interactive functions between it and other PWA's before making any adjustments.

16-4. Video Processor Encode/Decode Alignment

NOTE

Use of the Video Processor requires that jumper J2 on the motherboard be removed.

1. Use tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN.

2. Carrier decode and sample pulse alignment:

   a. With power off extend the video Processor PWA.

   b. Connect oscilloscope to U1-12 and trigger internally.

   c. Set jumper J1 to position A–B and set jumper J2 to position B–C.

   d. Adjust R7 (3.58-MHz) symmetry for a symmetrical square ware.

   e. Connect oscilloscope to TP5 and trigger internally.

   f. Adjust L1 (decode subcarrier peaker) for maximum 3.58-MHz signal (1.4 Vp-p or greater).

   g. Connect channel 1 of oscilloscope to TP3 and connect channel 2 to TP8. Trigger from pin 49 (REF H drive).

   h. Adjust R34 (burst sample center) so that sample pulse at TP3 is centered in burst area of decoded video at TP8.

   i. Adjust input test generator subcarrier phase so that decoded burst at TP8 is at zero volts (blanking level).

   j. Connect oscilloscope to TP4 and trigger from pin 49.

   k. Adjust R12 (offset) for +4.0 (±0.5) Vdc. If this level cannot be obtained, place jumper J1 to position B–C, turn power switch on, and readjust R12 for 4.0 (±0.5) Vdc.

   l. Return jumper J2 to position A–B.

   m. Adjust R41 (decode subcarrier phase centering) for 4.0 (±0.5) Vdc.

3. Decode/encode alignment:

   a. Connect 75% color-bar test signal at standard level to TAPE VIDEO IN connector.

   b. Connect oscilloscope to TP8 and trigger from pin 49 (REF H drive).

   c. Adjust oscilloscope to display a transition of chroma.

   d. Adjust L4 (R–Y decode filter) and L5 (R–Y decode filter) for flat base and smooth transition. (L4 adjusts transition and L5 adjusts amount of ringing or ripple.)

   e. Connect oscilloscope to TP10 and trigger from pin 49.

   f. Adjust oscilloscope to display a transition of chroma.

   g. Adjust L10 (B–Y decode filter) and L11 (B–Y decode filter) for flat base and smooth transition. (L10 adjusts transition and L11 adjusts amount of ringing or ripple.)

   h. Connect oscilloscope to TP15 and trigger from pin 49.

   i. Position jumper J5 to A–B and J4 to B–C.

   j. Adjust R104 (B–Y balance) for minimum subcarrier on blanking and sync tip.

   k. Position jumper J5 to B–C and position jumper J4 to A–B.

   l. Adjust R53 (R–Y balance) for minimum subcarrier on blanking and sync tip.

m. Position jumper J5 to A–B.

n. Adjust L13 (encode quadrature) and R57 (R–Y gain) for minimum subcarrier beat on the lower edge of the cyan burst.

o. Adjust R162 (clamp dc level) for zero (±0.1)V at blanking level.

16-5. Video Processor System Adjustment

1. Connect a 75% color-bar signal at standard level to TAPE VIDEO IN.
2. Connect vectorscope channel A to TP15 and trigger vectorscope internally.
3. Switch test signal sync generator R–Y signal to OFF.
4. Adjust vectorscope to place horizontal vector at 0° .
5. Switch sync generator R–Y to on and B–Y to off.
6. Adjust L3 (decode quadrature) for a vertical vector display 90° from that in step 4.
7. Switch sync generator B–Y to ON.
8. Adjust L17 (chroma peaker) for maximum chroma.
9. Adjust L2 (encode subcarrier frequency) for minimum chroma jitter.
10. Connect vectorscope channel A to MONITOR VIDEO OUT connector. Trigger vectorscope internally.
11. Connect a waveform monitor channel A to MONITOR VIDEO OUT (use loop-through capability of vectorscope). Trigger monitor internally.
12. Alternately select NORMAL and positions of reference sync generator switch S1 and adjust the following for the same indications in position that occur in NORMAL position:

    a. R35 (chroma level) for identical chroma.

    b. R162 (clamp dc level) for identical blanking.

    c. R181 (luminance level) for identical luminance.

13. Return S1 to its operational position, and return PWA to its slot.

16-6. Chroma and Luminance Filter Alignment

Filter alignment is a factory adjustment requiring a video sweep generator and spectrum analyzer and is given here for reference only. Do not attempt adjustment without the required test equipment. The filter alignment would normally be done between steps 2 and 3 of paragraph 16-5.

1. Carefully unsolder shielded cable signal and ground lead connected to E1 and E2, respectively. See component locator.
2. Connect video sweep generator output leads to E1 and E2.
3. Adjust sweep generator output level for 2.0 Vp-p.
4. Connect a spectrum analyzer to TP16 and sync to sweep generator output signal.
5. Position the following jumpers to position B–C: J4, J5, J6, J7, J10, and J11.
6. Adjust L12 (luminance low-pass filters) for a null at 3.671 MHz.
7. Adjust L14 (luminance low-pass filter) for a null at 3.488 MHz.

8. Connect a 0.01-μF capacitor between the junction of R130/L12 and the junction of T1/C81.

9. Position jumper J7 to A–B.

10. Adjust L19 (luminance low-pass filter) for a null at 1.576 MHz.

11. Position jumper J7 to B–C, and position jumper J6 to A–B.

12. Adjust T1 (luminance low-pass filter) for maximum 1.576 MHz.

13. Position jumper J6 to B–C, and position jumper J11 to A–B.

14. Adjust L20 (luminance low-pass filter) for a null at 4.301 MHz.

15. Position jumper J11 to B–C, and position jumper J10 to A–B.

16. Adjust T4 (luminance low-pass filter) for a null at 4.301 MHz.

17. Connect spectrum analyzer to TP9 and sync to sweep generator output signal.

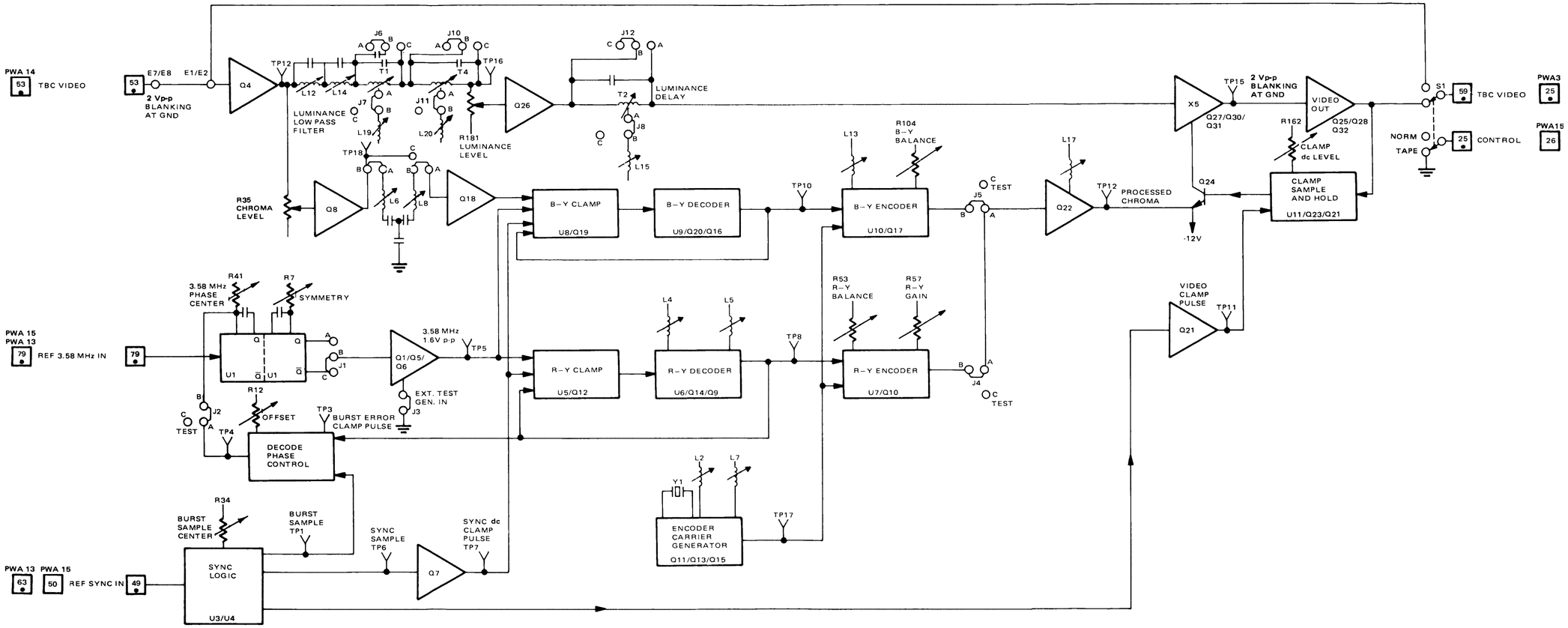
18. Adjust L6 (chroma band-pass filter) for a null at 2.000 MHz.

19. Adjust L8 (chroma band-pass filter) for a null at 7.16 MHz.

20. Reinstall the following jumpers to position A–B: J6, J7, J10, and J11.

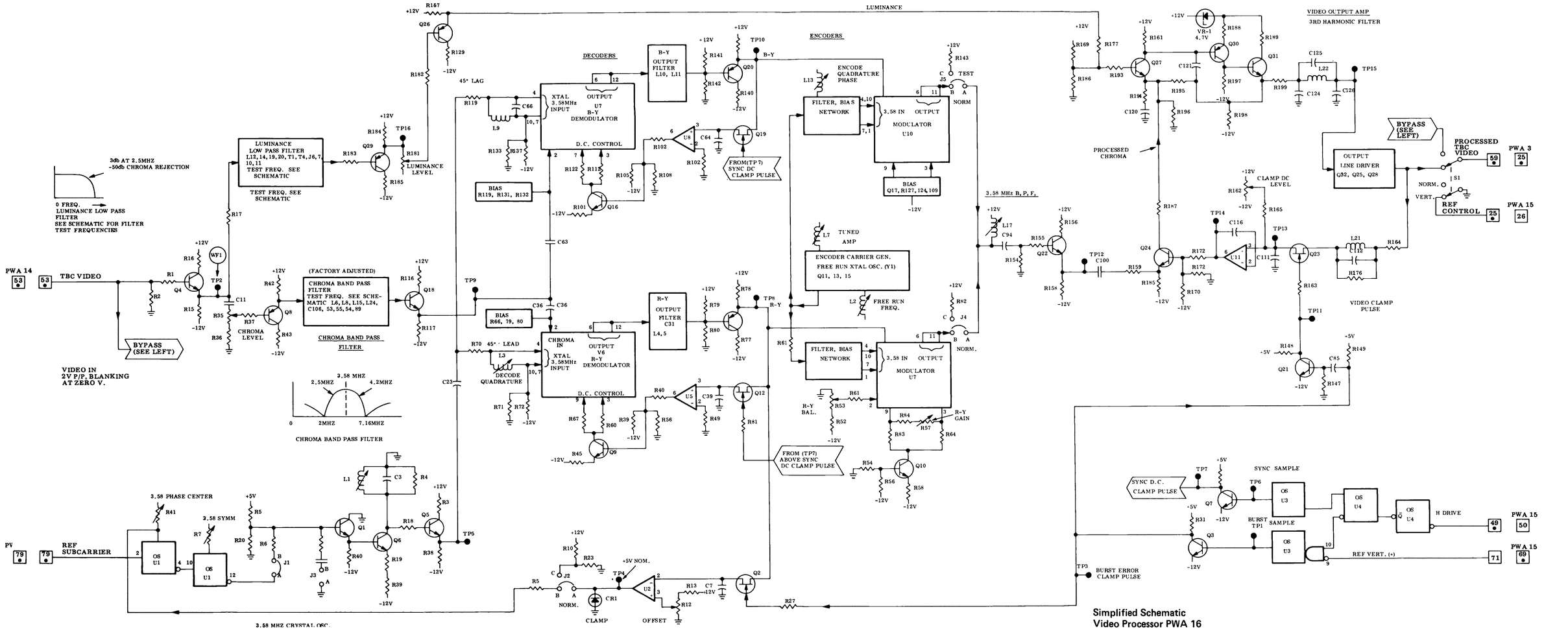
21. Remove the 0.01 μF capacitor connected in step 8.

22. Reconnect shielded cable disconnected in step 1. Center conductor goes to E1.



Block Diagram
Video Processor PWA 16
REFERENCE 1

PART II
16-7



Simplified Schematic
Video Processor PWA 16
REFERENCE 2

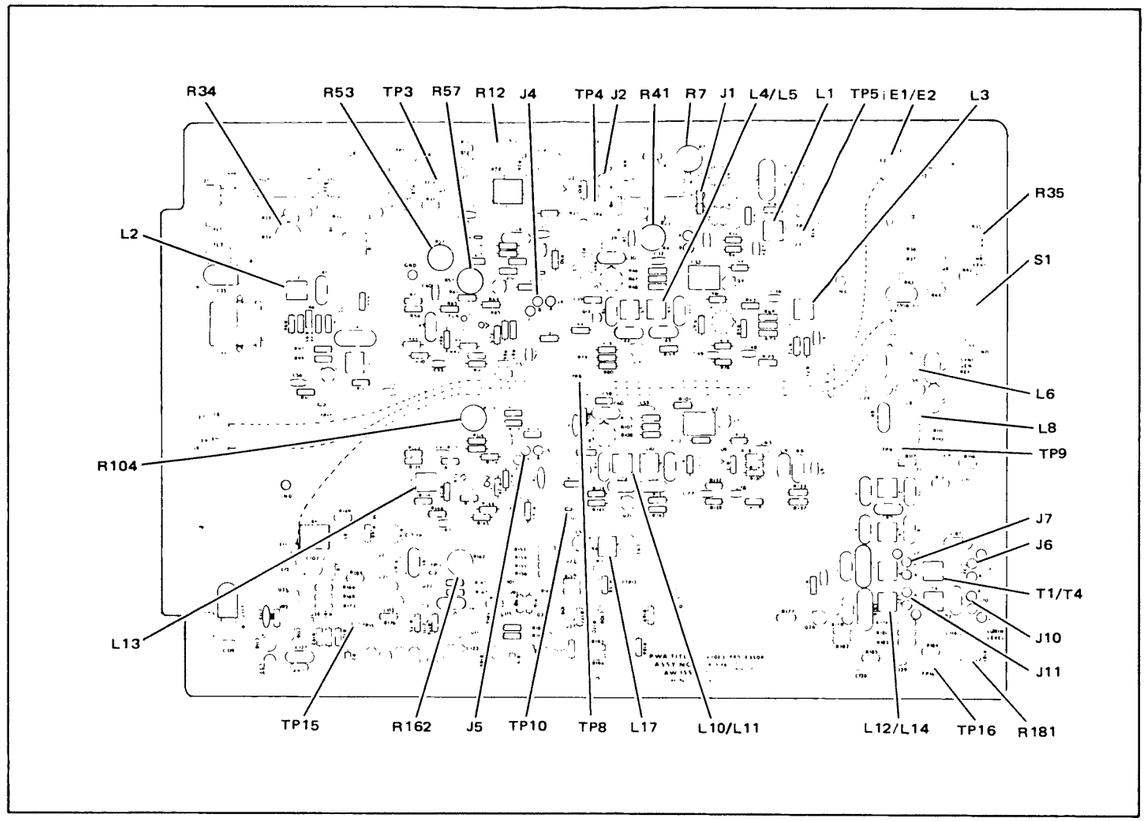
AMPEX 1809474-01

PWA 16 Adjustable Components

COMPONENT	FUNCTION	NOMINAL SETTING
R7	3.58-MHz symmetry	Adjust for 3.58-MHz symmetry.
R12	Offset	Adjust for 4.0 (± 0.5)V at TP4 with correct phase setting of J1.
R34	Burst sample	Sample pulse at TP3 should be centered in the burst area of the decoded video at TP8.
R35	Chroma level	Adjust for unity chroma gain as viewed on the vectorscope.
R41	3.58-MHz phase center	Adjust for 4.0 (± 0.5)V at TP4 with J2 in A–B.
R53	R–Y balance	Adjust for minimum subcarrier on blanking and sync tip.
R57	R–Y gain	Adjust for minimum subcarrier beat on the lower edge of the cyan burst; interacts with L13.
R104	B–Y balance	Adjust for minimum subcarrier on blanking and sync tip.
R162	Clamp dc level	Adjust for zero (± 100 mV) blanking level at TP15.
R181	Luminance level	Adjust for 2 Vp-p luminance level at TP15.
L1	Decode carrier	Adjust for maximum 3.58 MHz at TP5.
L2/L7	Encoder carrier generator	Adjust for minimum vector jitter.
L3	Decoder quadrature	Adjust 90° from burst phase with input R–Y off.
L4/L5	R–Y decoder output	Adjust L4 for flat baseline and L5 for minimum ripple.
L6/L8	Chroma band-pass filter	Null L6 at 2.000 MHz, L8 at 7.16 MHz.
L10/L11	B–Y decoder output	Adjust L10 for flat baseline and L11 for minimum ripple.
L12/L14/ L19/L20	Luminance low-pass filter	Null L12 at 3.671 MHz, L14 at 3.488 MHz, L19 at 1.576 MHz, L20 at 4.301 MHz.
L13	Encoder quadrature	Adjust for minimum subcarrier beat on the lower edge of the cyan burst; interacts with R57.
L17	Processed chroma	Adjust for maximum chroma at TP15.
T1/T4	Luminance low-pass filter	Peak T1 at 1.576 MHz; null T4 at 4.301 MHz.

PWA 16 Jumpers

JUMPER	POSITION – FUNCTION		JUMPER	POSITION – FUNCTION	
J1	A–D	0° decode subcarrier	J6	A–B	Normal
	B–C	180° decode subcarrier		B–C	Test – alignment of luminance low-pass filter
J2	A–B	Normal	J7	A–B	Normal
	B–C	Test – fixed phase to decode subcarrier		B–C	Test – alignment of luminance low-pass filter
J3	Removed	Normal	J8/J9	Not used	
	A–B	Test – external test generator input	J10	A–B	Normal
				B–C	Test – alignment of luminance low-pass filter
J4	A–B	Normal	J11	A–B	Normal
	B–C	Test – eliminates R–Y encoded chroma		B–C	Test – alignment of luminance low-pass filter
J5	A–B	Normal			
	B–C	Test – eliminates B–Y encoded chroma			



PWA 16 Component Locator

PWA 16 Component Locator

PWA 16 Test Points

TEST POINT	NAME
TP1	Burst sample
TP2	Video input
TP3	Burst error clamp pulse
TP4	Decode phase error
TP5	Decode subcarrier
TP6	Delay sync
TP7	Sync DC clamp pulse
TP8	R–Y chroma
TP9	Chroma
TP10	B–Y chroma
TP11	Video clamp pulse
TP12	Processed chroma
TP13	Clamp sample
TP14	Clamp error
TP15	Video out
TP16	Luminance
TP17	Encode subcarrier

Adjustable Components, Jumpers, Component Locator, Test Points Video Processor PWA 16 REFERENCE 3

PART II 16-9/16-10